



Electronics, Telecommunications and Information Technology

PhD THESIS

- ABSTRACT -

Theoretical And Experimental Research Regarding High-Performance Converters Used For Electric Vehicle Battery Chargers

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SUMMARY

It is well known that in the last decade, due to the need to preserve the environment, both in industry and in academia, considerable efforts have been made to replace conventional energy sources with renewable energy sources (also known as "green" energy sources). This trend has also influenced the automotive industry, as electric vehicles (EVs) are beginning to acquire an increasingly significant share of the market. For example, in 2019 in Norway 56% of new vehicles sold were electric, in Iceland they reached 24.5%, and in the Netherlands 15% [1].

Among the main reasons why the sales increase of EVs isn't steeper are the range, which is still below the range of internal combustion vehicles, the charging time, the charging infrastructure which is still underdeveloped and the price. However, these shortcomings open a wide front of research that aims to improve the capacity of batteries, increase their usage efficiency, reduce charging time or optimize the energy distribution system to cope with the simultaneous charging of a large number of EVs [2-5]. The battery management system, the external chargers installed in charging stations, the on-board chargers of EVs, the electric traction systems or power distribution grids are all systems that require both hardware and control systems, usually digital, of constantly increasing complexity.

In order to ease and accelerate the development of control systems for electrical or mechanical equipment with a degree of complexity similar to on-board systems of EVs or the related charging infrastructure, Hardware In the Loop simulations have been proposed in literature (HIL) [6-11]. These involve the emulation of the physical components of a product to allow the design and testing of the control system in the absence of some of the system's hardware components. This approach to the development process allows the design of the digital control system in parallel or in advance of the product's power electronic (or mechanical) system design, reducing the total development time and providing an additional validation step besides conventional simulations. While conventional simulations allow virtual testing of the control system, HIL simulations can be used to test the control system in its final implementation. Also, through real-time simulators, HIL simulations allow testing the interaction between the control system and the controlled process. While for the development of various control systems related to the traction system of EVs many examples of HIL simulations can be found, the use of HIL simulations for the charging system is only marginally treated in literature. Also, the real-time simulation models of the converters commonly used in battery charger implementations are averaged models with a limited utility due to poor accuracy.

Another application of real-time simulators whose use has become more frequent with the increase of the performance-cost ratio of integrated digital systems is represented by monitoring or error detection systems where the real-time simulator runs in parallel with the physical system and the predicted quantities are constantly compared with the actual quantities, which allows for drawing conclusions regarding the operation state of the system [12]. For such systems, the real-time simulator must be optimized in terms of resources used, must provide a high degree of fidelity while applying generic design methods. This allows implementation on a wide variety of (embedded) platforms using a wide range of programming languages and techniques. The automated industrial methods for generating real-time simulators which have recently been developed cannot achieve the performance needed to emulate the behavior of converters in the charger structure. Thus, the development of original alternative methods for real-time simulator design and implementation that are intended to be applied in monitoring or error detection systems is required.

Recently developed devices based on silicon carbide (SiC) [or] gallium nitride (GaN) allow an increased efficiency of converters in the structure of battery chargers enabling increased switching frequency, thus reducing the amplitude of the characteristic waveforms' ripple and the size of the components (especially the magnetic ones). A higher switching frequency allows an increased cut-off frequency of the control loop, which further constrains the latency of the control system. To obtain accurate models, real-time simulators also require very low latencies. Furthermore, taking into account the complexity of the control algorithms used and the number of functionalities to be implemented in the digital system of an EV, programmable devices known as "Field Programmable Gate Array" (FPGA) are increasingly emerging as solutions in applications that require low computational latencies or need to integrate a large number of functions on a single device. While the use of FPGAs for rapid prototyping development platforms is already the norm, such devices are already being used in mass consumer products as well [14].

1. Introduction

1.1. Objectives

Given the increasing complexity of digital control systems related to the charging and battery management functions described previously, the increasing interest in the use of FPGA devices both in the development phase (for rapid prototyping) and in production, this thesis aims to design a hardware platform and a procedure to help reduce costs, increase reliability, integrate, accelerate and facilitate the development of the battery charging and management system. Achieving this ultimate goal involves the following distinct objectives:

1. Develop a mathematical model of the power converters used for the implementation of the EV battery charger.
2. Develop an automated procedure for dimensioning the EV's battery charger control system coefficients.
3. Study the particularities of FPGA devices in the context of switch mode power supplies control system implementation and develop techniques to maximize the performance of these devices in such applications.
4. Determine the optimal FPGA programming techniques for each element of the architecture and highlight the advantages but also the limitations of high-level synthesis programs.
5. Implement a mixed signal platform to run relevant time and frequency domain identification methods for the power converters and the compensator in open loop or in closed loop. The purpose of this platform is to allow the compensator to be quickly and accurately tuned.
6. Develop a real-time simulator for the converters in the charger structure.
7. Develop a platform that allows the parallel operation of real-time simulation models with the reference converter and their characterization in time and frequency domain either individually or comparatively. Thus, an emphasis will be laid not only on the use of the real-time simulator in HIL type simulations, but also in error detection systems in order to increase system reliability.
8. Design an integrated battery management and charging system based on wireless communication that demonstrates the versatility and capability of hybrid ZYNQ devices to reduce the number of system devices by implementing a large number of functions that require high-performance digital support in a single device and also the

ease interfacing with other EV systems. These features can help reduce the complexity and the size of the management and control platform and increase its flexibility and reliability.

1.2. Methodology

The methodology applied for the study proposed in this thesis consists in developing a mathematical model for the power and control circuits necessary to implement an EV battery charger, designing an automated method of design based on the given input parameters, validation by simulations, the implementing the digital structures on FPGA and, finally, validating of the developed systems experimentally. Experimental validation involves measuring the time and frequency response of the converters in the charger structure (both open loop and closed loop) using the designed innovative platform, comparing the experimental results with the ideal ones obtained by simulation and performing a comparative analysis between the reference converter and the real-time simulator developed. This last step proposed for experimental validation presumes that the real-time simulator and the reference converter operate in parallel using the same input quantities. Thus, the outputs of the two blocks can be tracked simultaneously.

2.3. The structure of the thesis

The chapters of the thesis follow the validation of the proposed methods, from the development of the mathematical models of the converters to the validation of the real-time simulator demonstrating an its use case exemplification. The first chapter presents an analysis of the current state of knowledge, defines the objectives of the thesis and the methodology used to obtain the results. The issues approached in this chapter include theoretical aspects related to battery management, charger structure, types of converters, control methods and real-time simulation techniques that can be applied to emulate charger power stages. Chapter 2 presents the analysis of the converters selected for the implementation of the charger, while the control techniques applied and the implementation of the charger's control system on FPGA are discussed in Chapter 3. The real-time simulation of the charger is presented in Chapter 4. The contributions for increasing the efficiency of the battery management and charging system are presented in Chapter 5, and the interpretation of the results along with the final conclusions are presented in Chapter 6.

2. Study 1 – Analysis Of The Power Converters Used For The Implementation Of The Electric Vehicle On-Board Charger

2.1. Introduction

EV on-board chargers are subdivided into 3 categories: Level 1, Level 2, and Level 3 chargers. The first 2 categories can provide output powers up to around 2kW and are located on-board of the vehicle. Rapid chargers (Level 3) can provide up to 350kW and are external. The typical structure of an EV charger consists of 2 stages: an AC-DC stage and a DC-DC stage. The AC-DC stage is powered directly from the supply grid and is designed to convert the input voltage into a DC voltage, to ensure power factor correction and to limit the the harmonics of the currents injected into the grid [15, pp 190-203]. The DC-DC stage is designed to ensure

galvanic isolation and to implement the charging method: constant current (CC), constant current – constant voltage (CC-CV), multistage constant current (MCC), etc.

Because this thesis primarily focuses on accelerating the development of the digital control system of on-board EV chargers (Fig. 1) by designing innovative methods for characterizing power converters using, among others, real-time simulation, the most frequently used topologies in these types of applications were selected to illustrate the concepts. For the AC-DC stage the typical implementation based on the Boost converter (Fig. 2) supplied from a single-phase system was selected, while for the DC-DC stage an implementation based on the Phase Shift (PS) converter (Fig. 3) was adopted.

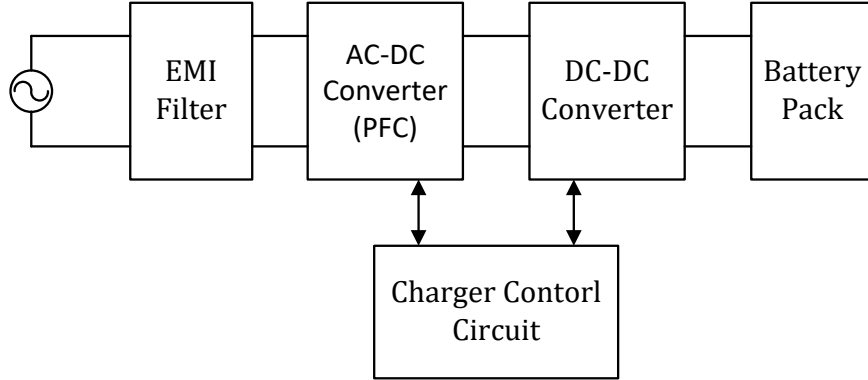


Fig. 1: Block diagram of a battery charger [17]

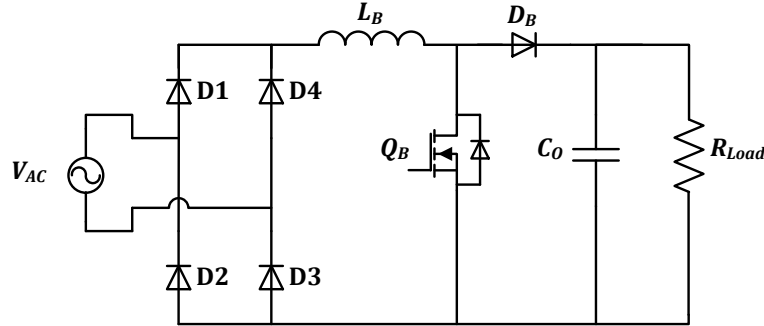


Fig. 2: AC-DC stage based on conventional Boost topology [18]

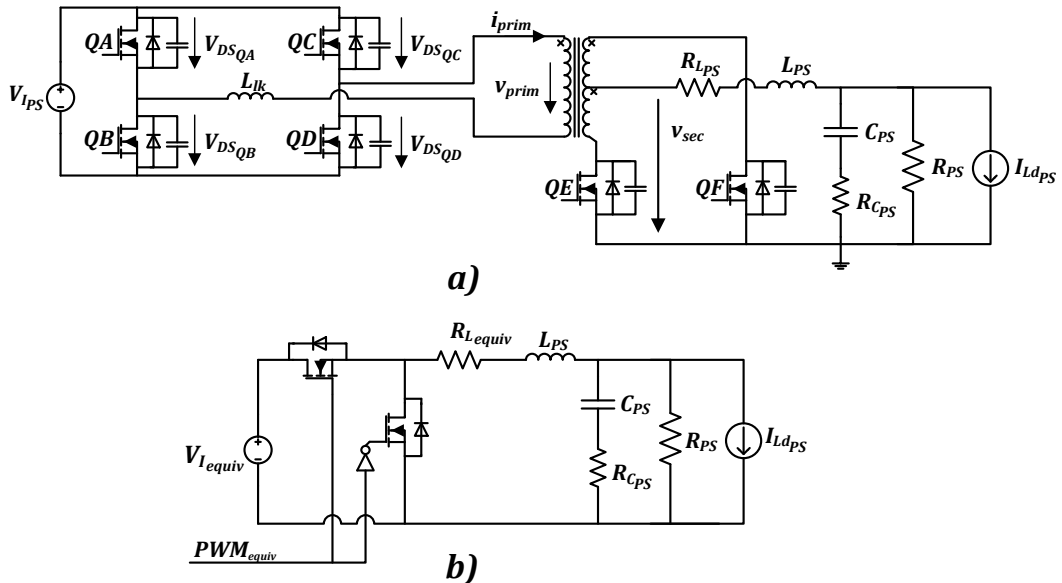


Fig. 3: a) DC-DC stage based on PS topology, b) Ps converter equivalent model [19]

Although the main criterion for choosing the topologies used was to accommodate as many applications as possible, a detailed comparative analysis was performed for the numerous variations of the Boost, Boost Interleaved and Bridgeless Boost topologies that may be used for the AC-DC stage and for PS and LLC topologies for the DC-DC stage[16].

2.2. Working hypothesis / objectives

The objectives of the study proposed in this chapter are:

1. Defining a procedure for dimensioning the power converters for the AC-DC and DC-DC stages of the battery charger.
2. Defining a procedure for estimating the efficiency of the AC-DC and DC-DC stages.
3. Simulation of the topologies chosen in order to obtain the reference waveforms to be compared with the results obtained by real-time simulation of the battery charger.
4. Obtaining the averaged and discrete small signal models for the design of the battery charger's analog and digital control systems.

2.3. Method

The analysis proposed for the selected topologies consists of the estimation of the steady state currents and voltages waveforms in order to evaluate minimum, peak, average, and RMS values required for generating the bill of materials and estimating of the dissipated power. The steady state analysis is followed by the small-signal analysis. For this purpose, two methods were proposed. The first method, based on averaging, was applied in designing the analog control of the battery charger. The second method is used to determine the discrete domain transfer functions of the converters used for the two stages of the charger and represents the basis for the digital control design.

2.4. Results

The validation of the developed mathematical models was achieved through simulation. The reference waveforms used for the validation of the real-time simulator of the battery charger were obtained through the same means (PSIM was the main simulator used for this purpose). The waveforms (currents through the inductor, through the output capacitance, through the diode, and through transistor, the output voltage, the diode reverse voltage drop, and the transistor drain-source voltage) specific to the AC-DC stage that characterize the behavior at the mains supply frequency are shown in Fig. 4, while the waveforms describing the behavior at the switching frequency are presented in Fig. 5.

The waveforms (currents through the inductance of the output filter, through the output capacitance, through the transistors of the primary and secondary rectifier bridge, the output voltage and the voltage drop across the switching elements) characteristic to the DC-DC stage are shown in Fig. 6.

The transfer functions that characterize the small signal model obtained numerically by running the developed MATLAB scripts are illustrated in Fig. 7 - Fig. 10. Their corresponding Bode plots are presented comparatively, both the transfer functions obtained with the state space averaging method and those corresponding to the discretized small signal model being illustrated.

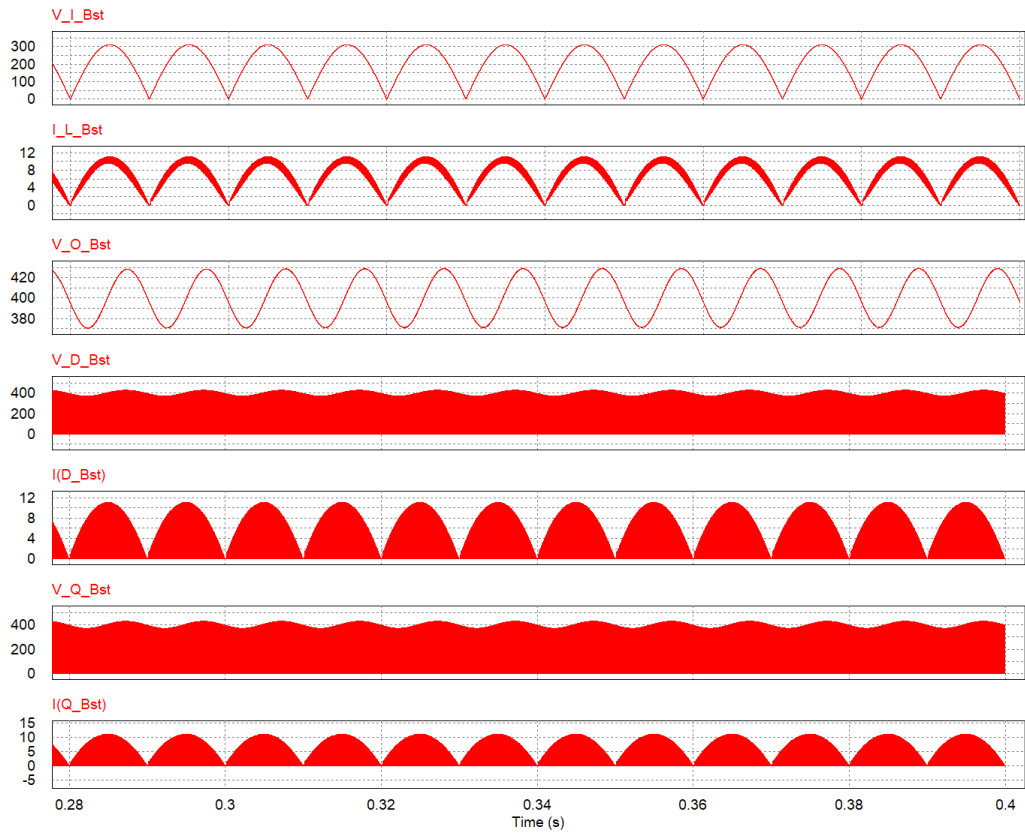


Fig. 4: The characteristic waveforms of the AC-DC stage at low (mains supply) frequency behavior



Fig. 5: The characteristic waveforms of the AC-DC stage at the switching frequency

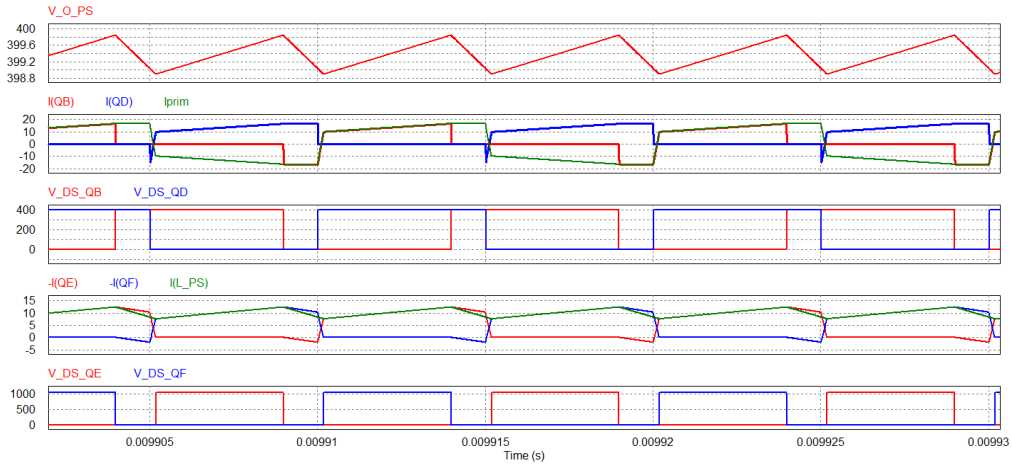


Fig. 6: The characteristic waveforms of the PS converter in steady state

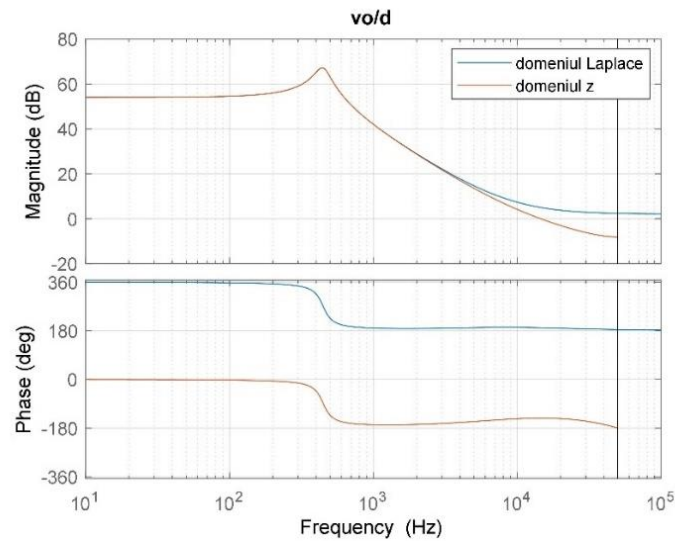


Fig. 7: Bode diagram of the transfer function that models the variation of the output voltage of the Boost converter depending on the variation of the duty cycle

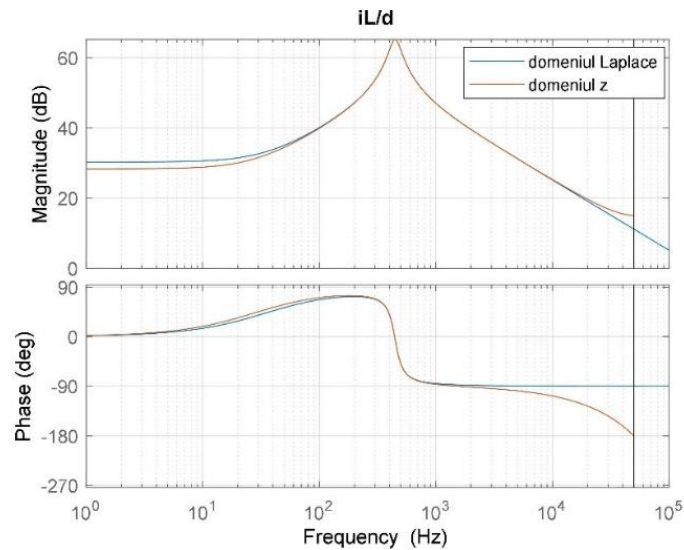


Fig. 8: Bode diagram of the transfer function that models the variation of the current through the inductance of the Boost converter depending on the variation of the duty cycle

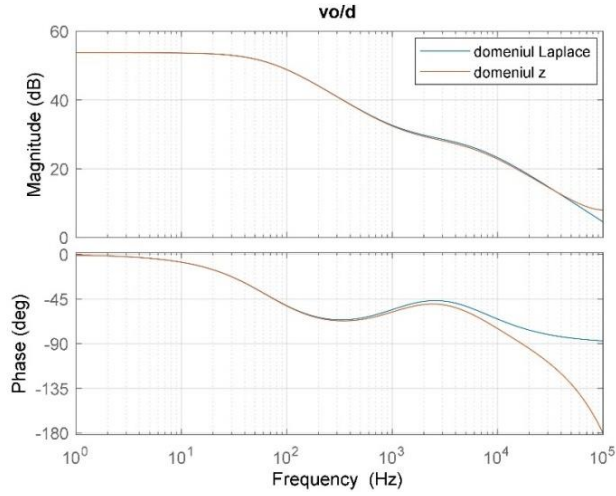


Fig. 9: Bode diagram of the transfer function that models the variation of the output voltage of the PS converter depending on the variation of the duty cycle

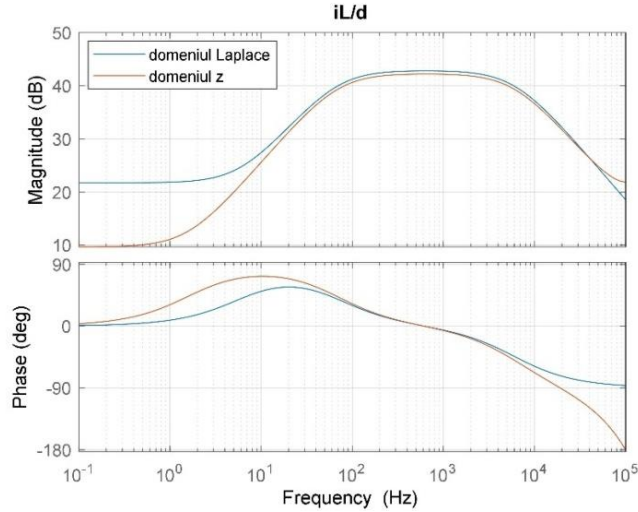


Fig. 10: Bode diagram of the transfer function that models the current variation through the inductance of the PS converter depending on the variation of the duty cycle

2.5. Discussions

The design of the AC-DC stage based on the Boost converter is well described in literature, all aspects necessary for circuit dimensioning, the modeling of the stationary regime and the small signal model being well described. In the case of the topology chosen for the PS converter, an additional analysis of the steady state was necessary to describe the current and voltage waveforms across the elements of the primary side bridge and of the rectifier in the secondary side. A more accurate analysis than the one available in literature was also performed for the RMS values of the currents through the switching elements.

From a wider range of methods for obtaining the small signal model of the converters used, two were chosen. The state space averaging method was used to derive the relevant transfer functions in the Laplace domain and a discrete one was used to describe the relevant transfer functions in the z-domain. The reason for choosing these methods is their ease of use, both being formal methods. While average-based methods can be derived analytically relatively straightforward and no specialized programs are needed to obtain the transfer

function coefficients, the discrete method presented is not practical in the absence of a numerical specialized tool. For a large number of applications average-based methods are sufficient, but if specialized programs (e.g. MATLAB) are used, both methods present a similar degree of difficulty.

3. Study 2 - Control Of Electric Vehicle On-Board Charger

3.1. Introduction

As this thesis focuses especially on adapting and accelerating the development process of FPGA based control systems required for EV battery chargers (especially on-board chargers), conventional control methods were applied to illustrate the presented concepts.

The control system ensures the basic functionality of the two stages of the on-board charger. The principle diagram of the control system of the AC-DC stage is shown in Fig. 11.

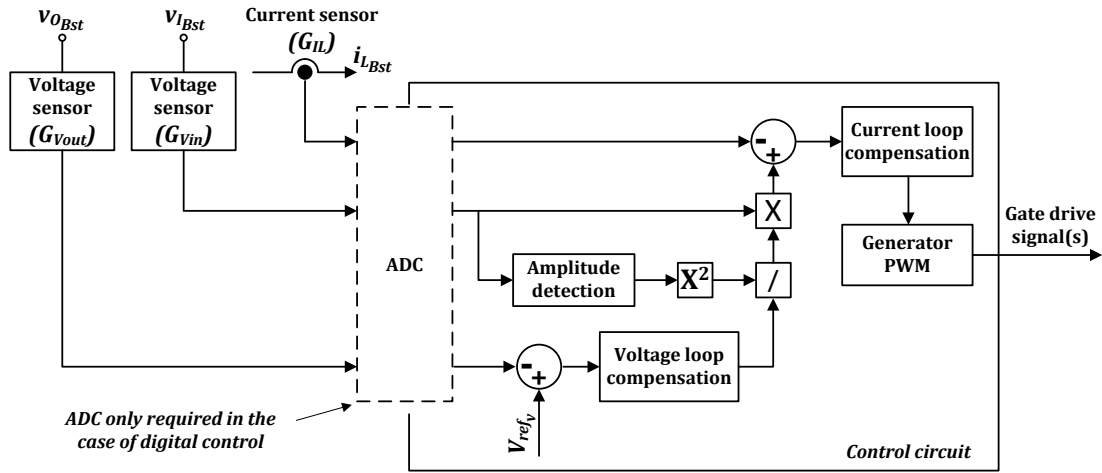


Fig. 11: AC-DC stage control

The role of the DC-DC stage, in addition to ensuring galvanic separation, is to implement the battery charging method. The most widely used charging method, also selected for the system presented in this thesis as an example, is the CC-CV method. The schematic diagram of the DC-DC stage control system is shown in Fig. 12 [20].

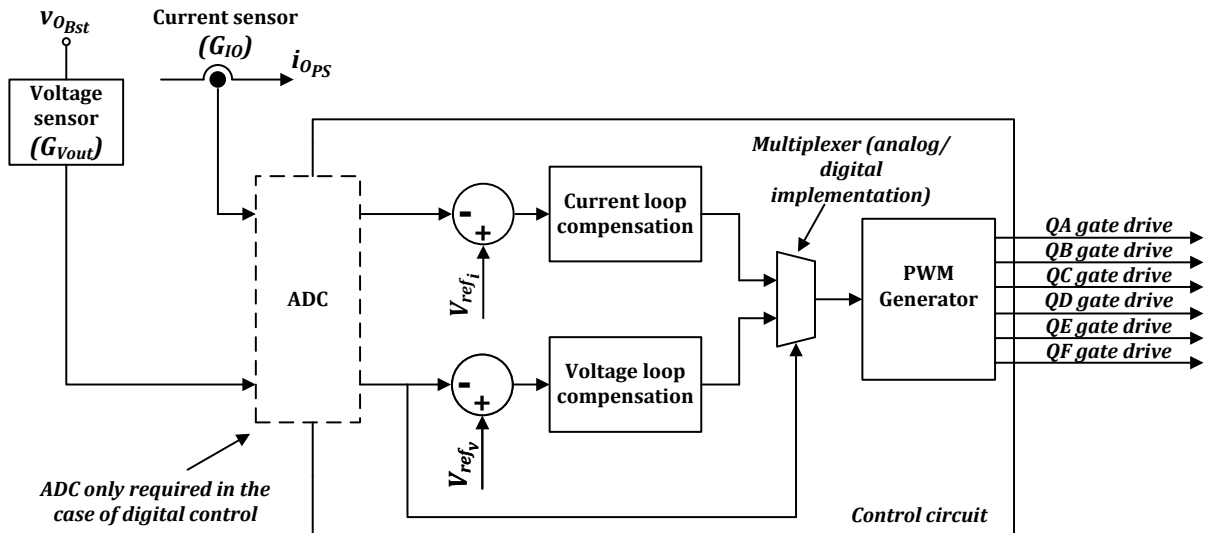


Fig. 12: DC-DC stage control

Considering that one of the objectives of this thesis is to implement the control system of the EV battery charger on an FPGA device, the analysis of the particularities of these devices revealed a series of shortcomings that are characteristic in this application: insufficient performance of the analog to digital converters (ADCs) integrated at the FPGA level, lack of dedicated PWM generators, and difficulty of programming.

3.2. Working hypothesis / objectives

The main purpose of this chapter is to minimize the shortcomings of the above-mentioned FPGA devices in digital control applications. The steps taken to achieve this goal are:

1. Design, simulate and implement on a FPGA device the control system of the AC-DC and DC-DC stages of the EV on board battery charger.
2. Highlight the limitations of FPGA devices and identify methods to maximize the performance of both the compensator and the discrete PWM generator.
3. Establish a development process based on a high-level synthesis tool to accelerate the implementation of the control system on FPGA by finding the optimal compromise between development time, performance, flexibility, resource utilization and ease of controlling the usage of the FPGA device primitives.
4. Develop a hardware system that exploits the benefits of the FPGA as a development platform while adding to the control system the possibility to perform time and frequency characterization procedures of both the power converter and the control loop as a whole, designed to facilitate and to accelerate, in turn, the process of developing digital control.

3.3. Method

Among the disadvantages of the FPGA devices mentioned above, a first element addressed is the lack of a dedicated PWM generator. For this purpose, an original architecture was proposed to obtain the maximum resolution allowed by the speed of the output buffers of the FPGA, using a clock frequency as low as possible for the internal logic. The key to increasing performance is the use of the OSERDES primitive, which is the output stage of the FPGA that allows the maximum transfer rate. The proposed implementation opted for a parallel implementation. The outputs of 8 out-of-phase counters are compared simultaneously with the input, while the outputs of the 8 comparators are further serialized. The frequency ratio between the parallel and serial interface is 1:8. In order to illustrate the obtained performances, it is possible to choose, for instance, the generation of a PWM signal with the frequency of 100KHz and 13 bits of resolution. With the conventional architecture, the internal counter of the PWM generator should operate at the frequency of 800MHz, a value that is not allowed by the clock distribution network of the chosen FPGA. With the proposed architecture, the internal logic can operate at 100MHz, which represents a considerable advantage. The block diagram of the proposed generator is shown in Fig. 13 [21].

A second shortcoming of FPGAs for which solutions of minimization were proposed is the difficulty of programming. For this purpose, the opportunity to use high-level synthesis languages was analyzed. For both current and voltage loops of the AC-DC and DC-DC stages, the main elements of the control system implemented on FPGA are the compensators (PID controller) and the discrete PWM generator.

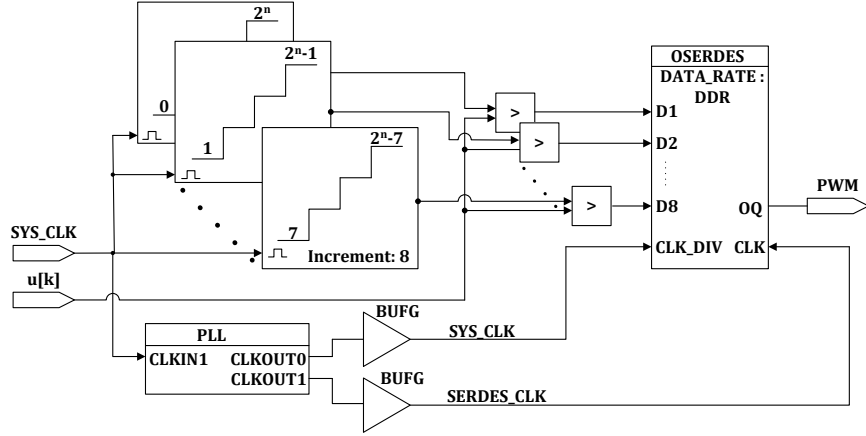


Fig. 13: Implementing the discrete PWM generator [21]

Because the compensator requires a series of arithmetic operations with operands represented as fixed-point values, its functionality is much easier to describe in C, where addition, subtraction, and multiplication are easily expressed, and conversions between various numerical representations are performed by "cast " operations. Since the Vivado HLS development environment supports input source files described in C, this was the choice for the development of the compensator. Vivado HLS provides the possibility to perform simulations in several stages of project development, the typical flow imposed by this programming environment being described in Fig. 14 [22]:

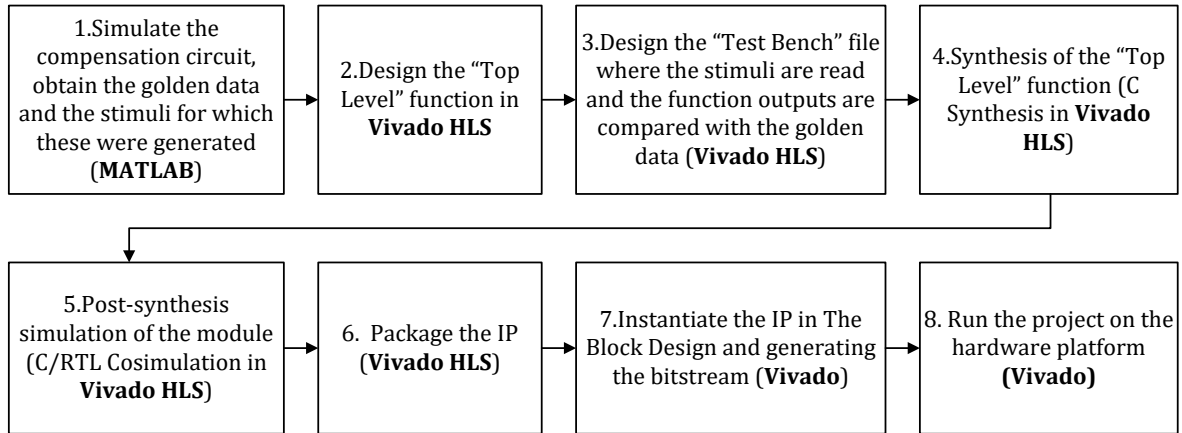


Fig. 14: Compensator development process based on Vivado HLS

However, the element with the most significant impact on facilitating and accelerating the development of the control system is the architecture of the proposed development platform (Fig. 15). In the first phase, to validate the development and characterization original methods, a Buck converter will be used (the evaluation board DM300023 provided by Microchip). The digital system is implemented on a hybrid ZYNQ device (XC7Z020) provided by Xilinx. The ZYNQ device is divided into two areas, one called the Processing System based on an ARM Cortex A9 processor with a wide range of peripherals available and one called Programmable Logic (PL) [23]. Because the PL consists of the typical structures of Xilinx 7 series FPGA devices, in the following the PL will be called FPGA. The Processing System helps to facilitate interconnection with other systems, but also to accept less restrictive tasks in terms of latency whose development is easier on the Processing System where conventional programming techniques can be used.

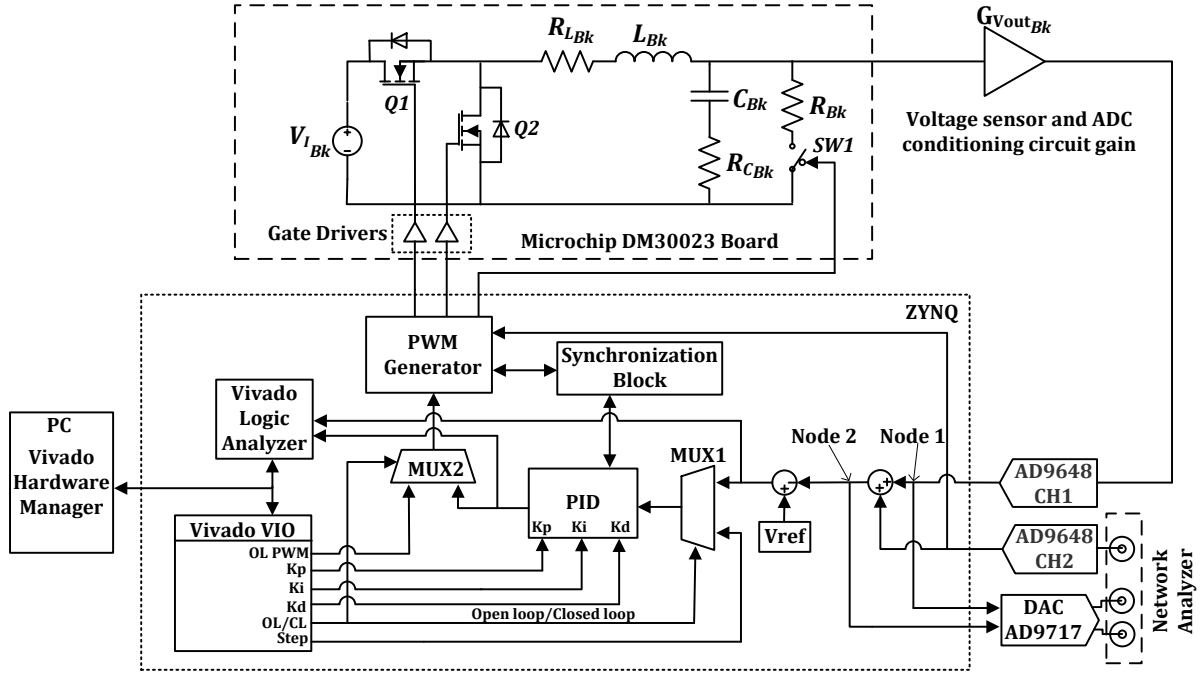


Fig. 15: Proposed development platform based on the ZYNQ XC7Z020 device [21]

A two-channel external ADC (AD9648) is used to monitor the power converter outputs but also to convert the disturbance signal generated by a network analyzer to digital format, providing an alternative to the conventional method of measuring the loop gain of the system. The main advantage of the proposed method is the elimination of the injection transformer and the resistance to be connected in series with the resistive divider in the feedback loop of the converter. Adding these components involves PCB modifications which can damage the circuit. Instead, the disturbance is introduced into the system using an ADC, while an AD9717 digital-to-analog converter (DAC) is used to convert the digital quantities before and after the insertion point of the disturbance into analog format allowing to visualize loop gain Bode plot using a network analyzer.

The voltage reference, the error amplifier, the compensator and the discrete PWM generator are all implemented in the FPGA. The interaction between the hardware system and the user is possible via two IPs provided by Xilinx: the logic analyzer (Integrated Logic Analyzer - ILA [24]) and the virtual input-output port (VIO - Virtual Input Output [25]) which, through a JTAG interface, communicates with the Vivado development environment (running on PC). The VIO IP will allow the user to change the operating parameters and the topology of the control circuit (by controlling several multiplexers) at run time. An alternative to this approach may be to employ the ZYNQ device Processing System to communicate with the PC, to enter system parameters and automatically compute the compensator coefficients. The logic analyzer provided by Xilinx includes an advanced trigger system that allows the visualization of any internal signal in the structure of the FPGA. The entire system, including the VIO and ILA IPs, runs over a single clock domain (100MHz) with no synchronization circuits between the blocks required.

The main advantage of the system shown in Fig. 15 is the ability to configure the circuit topology and the controller parameters without the need of reconfiguring the FPGA. Once the FPGA is programmed, the VIO IP can be accessed from the Vivado development environment interface, with MUX1 and MUX2 multiplexers being able to select the open-loop or closed-loop operation mode. In open-loop mode, the compensator will be isolated from the rest of the system, its inputs will be controlled by the VIO IP and its output will be connected to the logic analyzer. The discrete PWM generator will also have the inputs controlled by the VIO IP, its

output being a PWM signal with a constant duty cycle. The system allows the following validation steps:

1. Measurement of the frequency response of the power converter (in open loop).
2. Visualization of the PID controller's time domain response to a Heaviside step stimulus.
3. Plotting the system's loop gain with the loop closed.
4. Applying a load step to the closed-loop system and observing its time domain response.

3.4. Results

The experimental validation of the methods described in this section was performed using the hardware platform shown in Fig. 15. The first proposed validation step is to experimentally plot the frequency characteristic of the power converter. Such a measurement is useful primarily for validating the ideal mathematical model (plotted using MATLAB). For this purpose, a network analyzer can be used to generate a disturbance on channel 2 of the ADC and, by monitoring the output of the converter, the transfer function of the power stage can be displayed (Fig. 16). The frequency characteristic of the converter obtained experimentally is presented in comparison to the ideal, numerically modeled, characteristic. The network analyzer used was provided by the Analog Discovery digital oscilloscope, and the data collected by it were processed in MATLAB to represent on the same graph both the ideal and the measured characteristics.

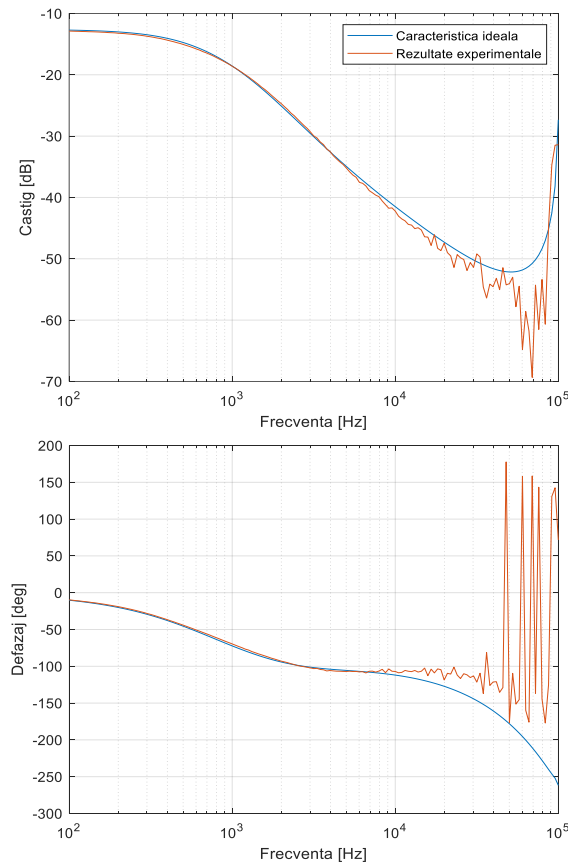


Fig. 16: Experimentally obtained Buck converter frequency characteristic [21]

The second validation step consists in the experimental validation of the compensator. For this purpose, the compensator response to a Heaviside step (generated by the VIO IP) can be visualized using the logic analyzer in the Vivado development environment (Fig. 17). It should be emphasized that, in this mode of operation, the compensator is completely isolated from the rest of the system and can be tested independently. Knowing the frequency characteristic of the power stage (obtained experimentally in the previous step), the derived mathematical model can be confirmed (or corrected) and the compensator parameters can be calculated to obtain the desired cutoff frequency and phase margin. In order to compare the result obtained after the implementation with the output of the ideal model, the result of the numerical model obtained in MATLAB was also presented (Fig. 18). It can be observed that the experimental results coincide with the numerical ones.

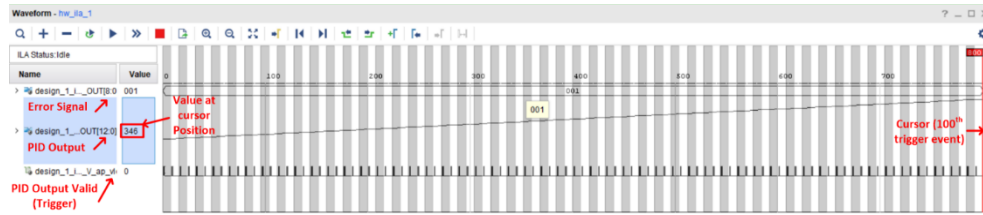


Fig. 17: Compensator step response viewed with logic analyzer [21]

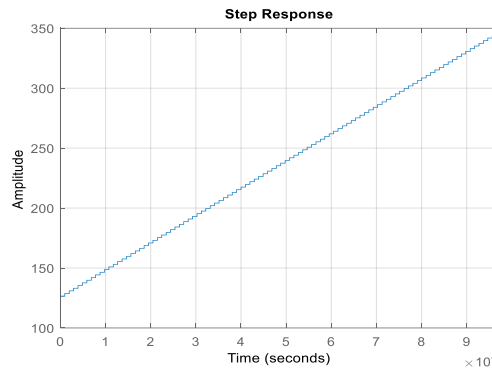


Fig. 18: The ideal compensator step response obtained in MATLAB [21]

Once the value of the compensator coefficients has been determined, the loop can be closed (MUX1 and MUX2 will select the closed-loop operation mode) with minimum risk of oscillations or unexpected errors. Because the stability of the system is theoretically evaluated by analyzing the open loop transfer function, plotting its Bode diagram is particularly useful. As presented in [26], this measurement can be made with the system operating in closed loop. The method proposed in this thesis will not use an injection transformer to introduce the disturbance into the system, instead one of the available channels of the ADC will be used. The output of the other channel of the AD converter, responsible for monitoring the output quantity, will be connected directly to the input of one of the channels of the DAC (Node 1 in Fig. 15). Node 2, which represents the superposition of the output quantity (voltage) of the converter and the disturbance, will be connected to the remaining free DAC channel. The network analyzer will evaluate the complex gain between Node 1 and Node 2, which actually represents the loop gain of the system [26]. The experimental and theoretical results are presented comparatively. Fig. 19 illustrates the ideal characteristic, the characteristic obtained with the conventional method of injecting the disturbance and the one obtained with the proposed method.

A final validation step that allows the analysis of the time-domain performance of the control loop consists in applying a load step by turning on switch SW1 and inserting the load resistance R_{Bk} in the circuit.

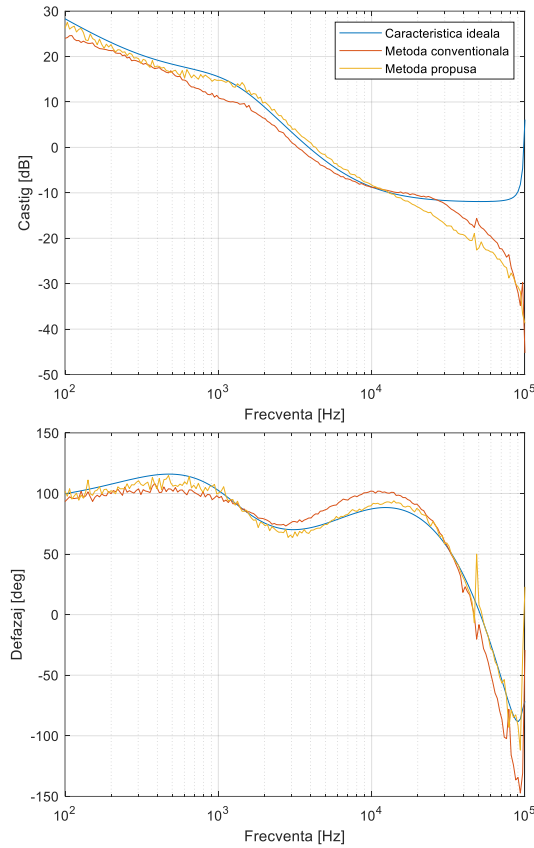


Fig. 19: Comparison between the conventional and the proposed methods of obtaining the loop gain

All these experimental validation procedures, as well as changing the compensator parameters, can be performed without reprogramming the FPGA device through the graphical interface of the Vivado programming environment. This largely eliminates the disadvantage of increased bitstream generation time and accelerates the development process. In addition to the validation process allowed by the development platform (a process that increases the degree of certainty when starting the system in closed loop and accelerates the validation of the control system), this is the second main advantage of the presented architecture.

3.5. Discussions

In this chapter, a procedure for designing the control system for an on-board battery charger of an EV with a special emphasis on digital control techniques was presented. For its implementation, a Xilinx 7 series hybrid device (ZYNQ XC7Z020) was chosen to implement the digital platform. The disadvantages associated with FPGA development, such as the use of less popular programming languages, the time-consuming development associated with low level design tools, synthesis and implementation times, or the need for in-depth knowledge of the internal structures of the FPGA have been eliminated by using an implementation flow based on the Vivado HLS development environment. Although the level of abstraction associated with Vivado HLS is high compared to conventional hardware description languages, it still allows effective control of the internal primitives of the FPGA, allows the choice of synthesis strategies aimed at reducing latency or reducing resources used and offers a wide range of interfaces that the developed module can use to interconnect with other blocks designed in FPGA.

The implemented hardware platform demonstrates the accuracy of the derived mathematical model and highlights the advantages of using FPGA technology in control systems. Beyond the much lower latency compared to DSP-based systems, the FPGA allows the use of a high-performance analog interface, being able to control several high-speed AD and DA converters in parallel. These converters were used to develop an original method for characterizing power converters and the control loop without the need to "break" the loop and use additional components. Along with the use of the Vivado HLS development environment, these elements contribute to the simplification and acceleration of the process of developing control systems on FPGA.

4. Study 3 – Real-Time Simulation Of The Electric Vehicle On-Board Battery Chargers

4.1. Introduction

The most widespread use cases of real-time simulators are HIL simulations and monitoring/error detection systems. Although for the implementation of real-time simulators the same methods used for offline simulators are adapted, a number of features specific to real-time simulators require a very different implementation process and the classification of methods according to performance also involves different criteria. A comparative analysis of ODE solvers from the perspective of implementing a real-time simulator, adapting HIL simulations for the battery charging system, and creating switched function models with a high degree of fidelity for the topologies used to implement the on-board battery charger are missing from literature, thus the results presented in this chapter contribute significantly to the originality of the thesis.

For the real-time simulation of switched mode power supplies, it is essential to obtain a simulation time step as small as possible. Unlike offline simulators where there is no direct relationship between the complexity of the circuit and the simulation time step, in the case of real-time simulators it is necessary to find an optimal compromise between the degree of simplification of the simulated circuit and the value of the simulation time step that can be obtained. A detailed model of the electrical components will not necessarily lead to more accurate results. If the additional computational effort introduced by a detailed model increases the simulation time step above a certain threshold, both the accuracy and the stability of the simulator will be altered. The behavior of a simulated closed-loop system will also depend on the value of the simulation step, as further proved in this chapter.

This chapter presents the steps taken to determine the optimal method for designing the real-time simulator and its implementation techniques. In order to validate and exemplify the utility of the designed real-time simulator, a platform (whose simplified block diagram is illustrated in Fig. 20) was developed based on the platform presented in the previous chapter. The platform is intended to allow: 1) the real-time simulator to operate in parallel with the reference converter 2) a comparative analysis between reference converter and real-time simulator through time and frequency domain measurements; 3) closing the loop either through the real-time simulator, illustrating the use of the real-time simulator in HIL systems, or through the reference converter, case in which the platform can operate as an error detection system. The reference converter and the real-time simulator will have common input signals.

4.2. Working hypothesis / objectives

The aim of this study is to develop a real-time, high-precision simulator of the EV's on-board battery charger that can be used successfully in both HIL-type simulations and error detection systems. To achieve this goal, the following steps are required:

1. Determine the optimal numerical solver for the system of equations (ODEs) describing the power converters.
2. Model the ripple of power converters for switching frequencies up to 200MHz.
3. Obtain a simulation time step below 100 ns.
4. Develop of a platform to highlight the performance and to exemplify the use cases of the real-time simulator.

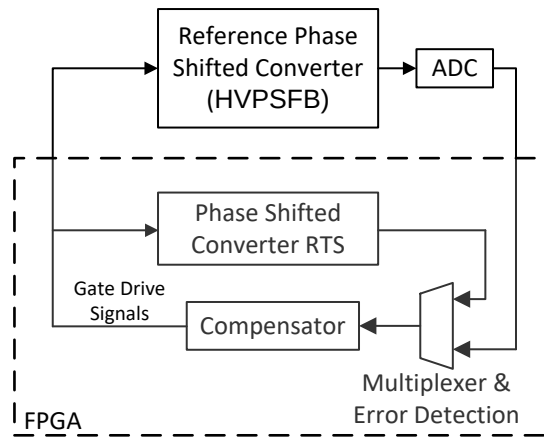


Fig. 20: Real-time simulator validation platform

4.3. Method

Given the necessary trade-off between the accuracy (complexity) of the models of the circuit elements and the value of the simulation time step, a system-level simulation was chosen, using a switched function model to develop the real-time simulator of the two stages of the EV on-board battery charger. A manual approach for modeling the circuits and for mathematically describe their behavior was proposed. More specifically, the state space equations representation (an ODE system) was used to describe the AC-DC and DC-DC stages power converters behavior. The switched function model of the Boost converter is illustrated in Fig. 21, and the implementation diagram of its real-time simulator obtained based on applying the AM1 method to its characteristic ODE system in Fig. 22. For the PS converter, the switched function model is illustrated in Figs. 23, and the implementation diagram of its real-time simulator is shown in Fig. 24.

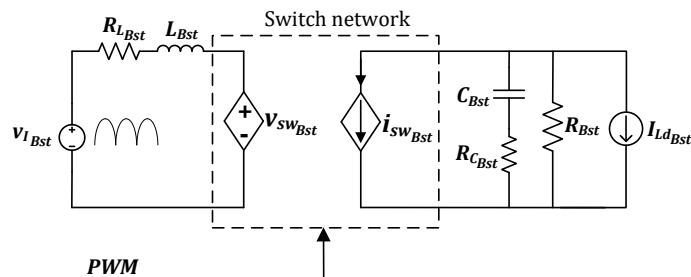


Fig. 21: The switched function model of the Boost converter

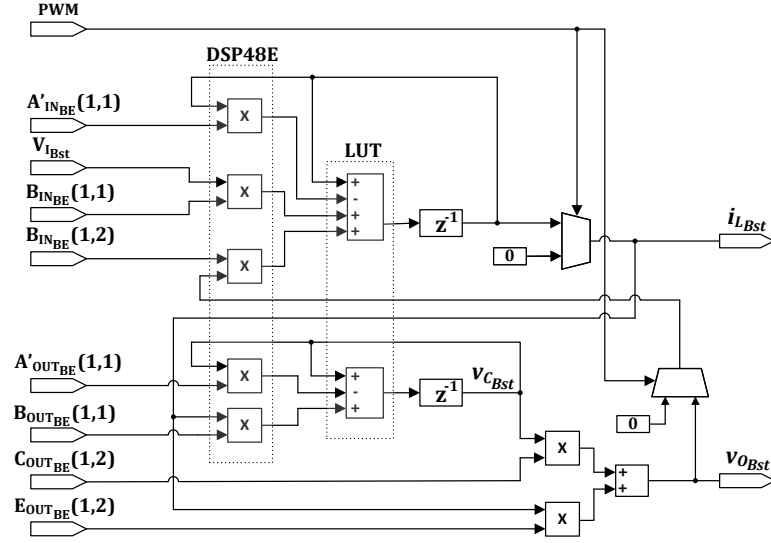


Fig. 22: Implementation of the real-time simulator of the Boost converter

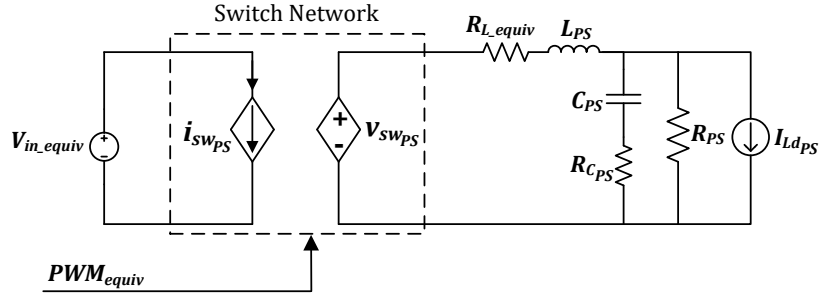


Fig. 23: PS The switched function model of the PS converter

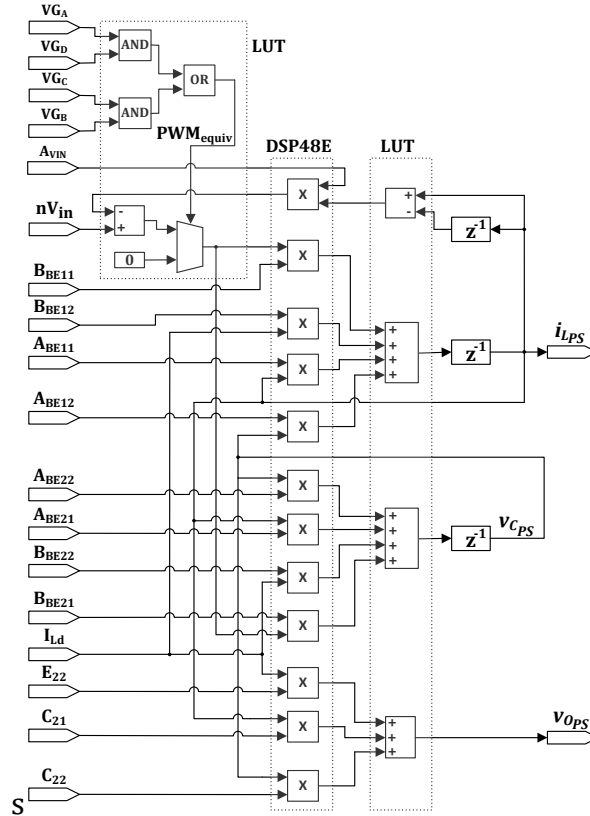


Fig. 24: Implementing the real-time simulator of the PS converter [27]

4.4. Results

The evaluation of the real-time simulator was performed at simulation level and experimentally. Thus, in a first stage, the results obtained by simulation means are presented (the circuit quantities tracked in these analyzes are the output voltage and the current through the inductance of the output filter), consisting of:

1) A comparative analysis of the steady state behavior between the idealized reference converter and the real-time simulator (Fig. 25).

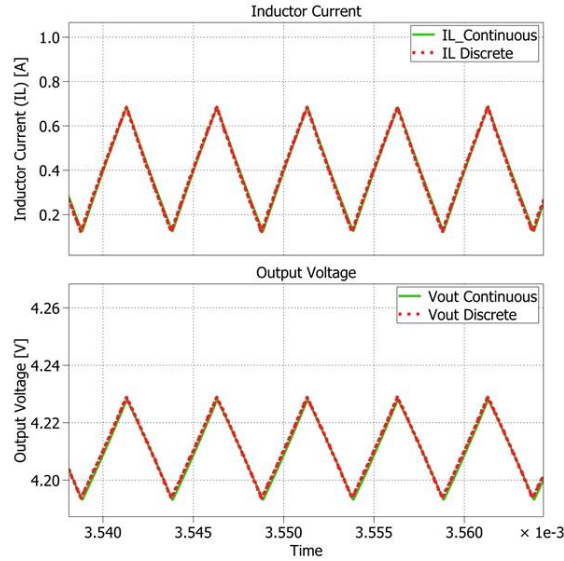


Fig. 25: The time domain output values predicted by the idealized model of the reference PS converter and the real-time simulator obtained by simulation (Plecs) [27]

2) The transient response corresponding to a phase shift increase from 0 to 90 degrees (Fig. 26).

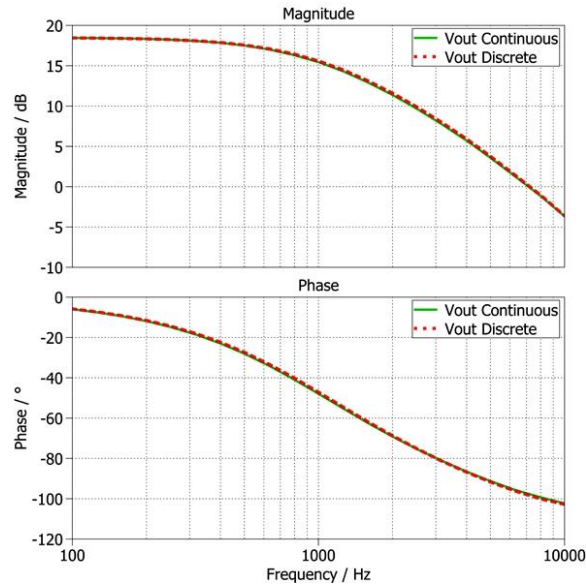


Fig. 26: Frequency characteristic of the idealized model of the reference PS converter and of the real-time simulator obtained by simulation (Plecs) [27]

3) A comparative analysis of the frequency response of the idealized reference converter and the real-time simulator (Fig. 27).

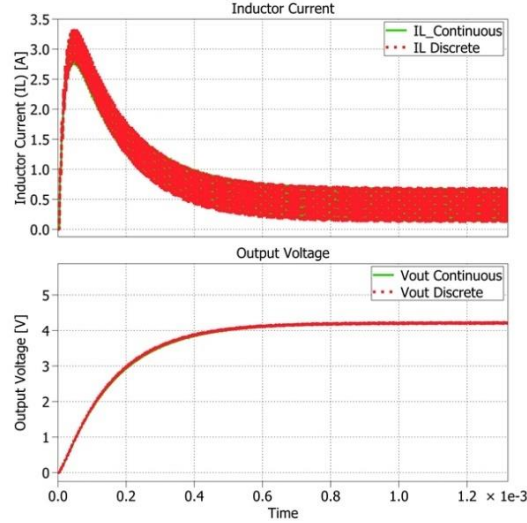


Fig. 27: Transient response of the idealized model of the reference PS converter and the real-time simulator obtained by simulation (Plecs) [27]

The experimental results obtained for the platform shown in Fig. 20 are divided into three validation steps. The first validation step represents a time domain and a frequency domain comparative analysis of the reference converter and its real-time simulator. To perform the time domain analysis (Fig. 28), the output voltage of the reference converter was first plotted. This was saved as a reference waveform on the oscilloscope's window (represented in green) and, subsequently, the output of the real-time simulator was displayed on the oscilloscope's channel 1 (represented in red). The two quantities were synchronized by using the QB transistor gate drive signal as trigger for both measurements. Although the reference converter and its real-time simulator operate in parallel and their outputs could have been viewed simultaneously, the alternated measurement of the output of the two blocks was chosen to avoid interferences between the oscilloscope channels.

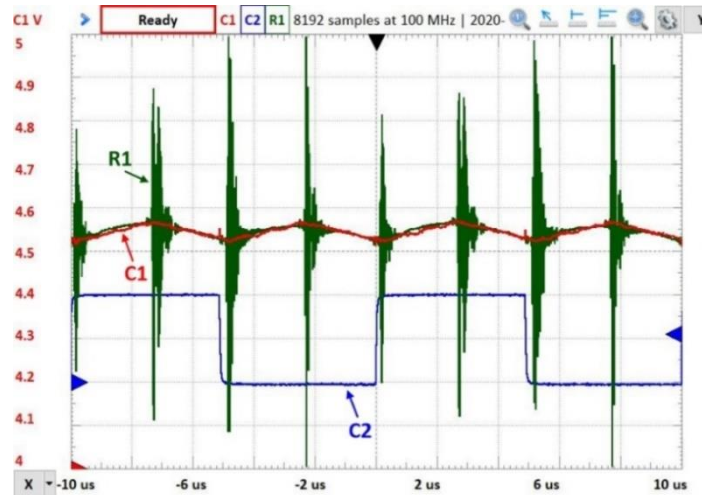


Fig. 28: Comparative analysis of the output voltage of the reference converter and the real-time simulator (horizontal scale: $2\mu\text{s}$ / div, vertical scale channel 1 and reference: 0.1V / div, vertical scale channel 2: 2V / div, offset channel 1 and reference : -4.5V , offset channel 2: -3V) [27]

The comparative analysis of the frequency response of the reference converter and its real-time simulator was performed similarly. First, the frequency response of the PS converter was plotted, it was saved as reference by network analyzer and, afterwards, the frequency characteristic of the real-time simulator was plotted. The results are shown in Fig. 29.

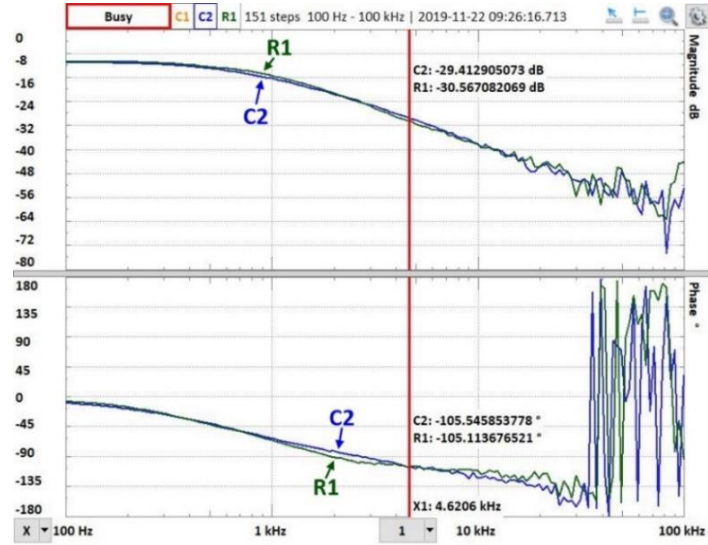


Fig. 29: Reference converter and real-time simulator frequency characteristic (experimental results)[27]

Another relevant experiment for the frequency domain analysis is a comparison between the loop gain of the reference system (with the loop closed through the reference converter) and the loop gain of the emulated system (with the loop closed through the real-time simulator). The element of the validation platform that allows switching between the two configurations is the MUX3 multiplexer. The results illustrated in Fig. 30 were obtained by first measuring the loop gain of the reference system (the reference 1 channel) and, afterwards, the loop gain of the emulated system (channel 2).

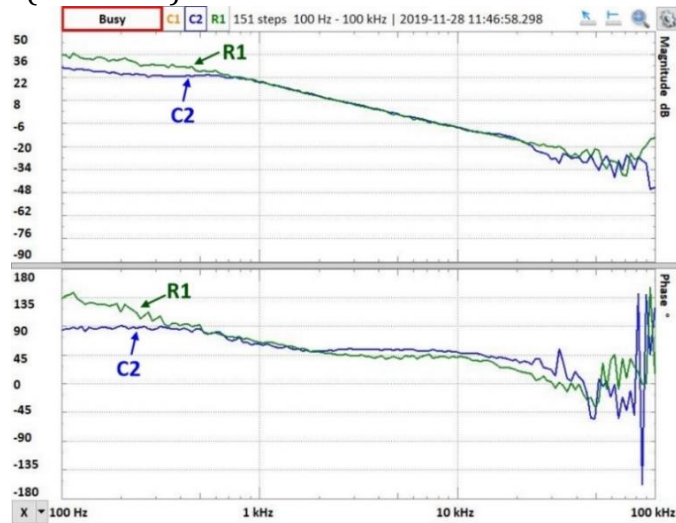


Fig. 30: Loop gain for reference and emulated systems (experimental results) [27]

The second validation step consists of a set of experiments (presented in Table 1) which aim to determine the ability of the real-time simulator to correctly predict the presence of limit cycling.

Table 1: The experiments proposed to determine the ability of the real-time simulator to model limit cycling

Experiment No.	N_{ADC}	N_{DPWM}	$N_{DPWMEff}$	Limit cycle existence condition
1	8	6	6	Satisfied
2	8	8	8	Not Satisfied
3	9	10	8	Not Satisfied

For the waveforms shown in Fig. 31, Fig. 32, and Fig. 33, channel 1 (red) represents the output voltage of the reference converter/real-time simulator and channel 2 (blue) the error signal. The results illustrated in Fig. 31 and Fig. 32 (experiment 1 and 2) demonstrate that, for discrete PWM generator resolutions below the maximum equivalent resolution, the real-time simulator accurately models limit cycling both in the presence and in the absence of its condition of existence. The results illustrated in Fig. 33 (Experiment 3) show that when the resolution of the discrete PWM generator is above the equivalent maximum resolution, it will exhibit a false condition for existence of the limit cycle.

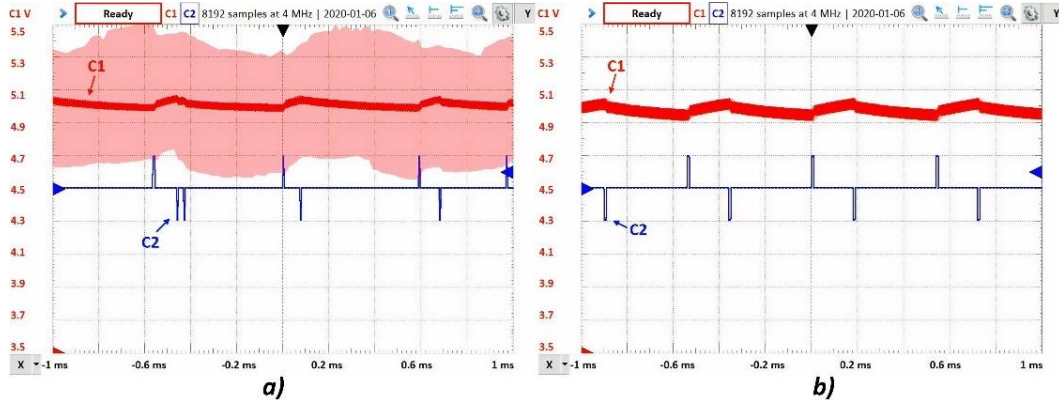


Fig. 31: The results of experiment 1 a) on the reference system b) on the emulated system (horizontal scale: $200\mu\text{s}$ / div, vertical scale channel 1: 0.2V / div, vertical scale channel 2: 1V / div, offset channel 1: -4.5V , offset channel 2: 0V) [27]

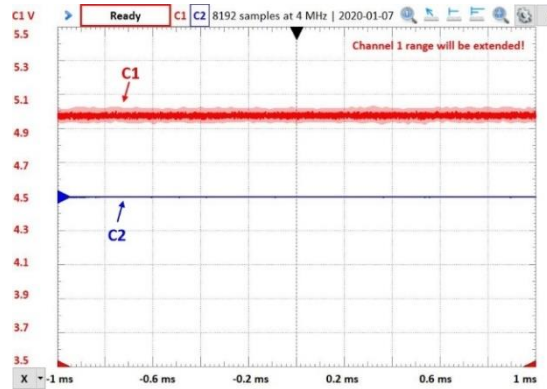


Fig. 32: Results of experiment 2 on the emulated system (horizontal scale: $200\mu\text{s}$ / div, vertical scale channel 1: 0.2V / div, vertical scale channel 2: 1V / div, offset channel 1: -4.5V , offset channel 2: 0V) [27]

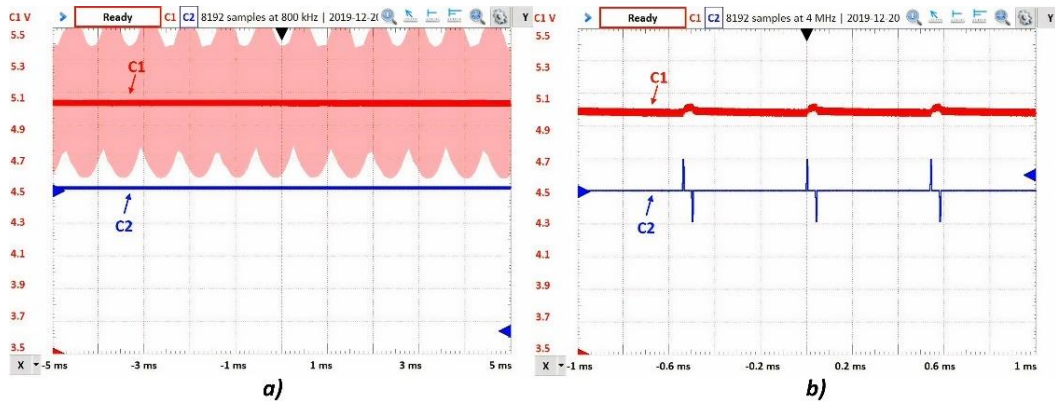


Fig. 33: The results of experiment 3 a) on the reference system b) on the emulated system (horizontal scale: $200\mu\text{s}$ / div, vertical scale channel 1: 0.2V / div, vertical scale channel 2: 1V / div, offset channel 1: -4.5V , offset channel 2: 0V) [27]

The last step proposed for the experimental validation of the platform is to overlap a step signal over the constant reference value. For this experiment the loop is closed (the reference converter being included in the loop) and the outputs of the reference converter and the real-time simulator are measured in parallel. The response of the reference converter (channel 1) and of the real-time simulator (channel 2) are illustrated in Fig. 34. Aging of components or other defects can be detected by comparing the two quantities.

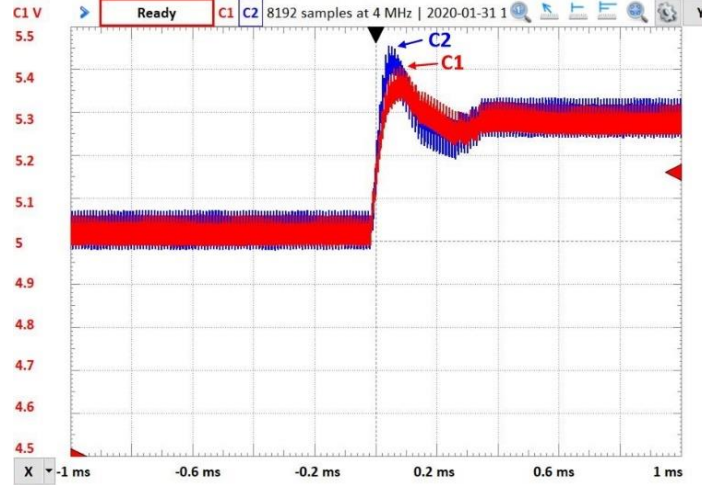


Fig. 34: Reference converter and real-time simulator response to a reference step perturbation (horizontal scale: 200 μ s / div, vertical channel 1 and 2 scale: 0.1V / div, offset channel 1 and 2: -5V) [27]

4.5. Discussions

The comparative analysis performed to determine the most efficient method of numerically solving an ODE system demonstrates that the choice of the optimal method is a compromise decided by several factors. Depending on the nature of the circuit considered, one method or another may be more efficient from case to case. Even though the proposed implementation method involves a manual process of circuit modeling, obtaining and discretizing the state space equations and generating the source code for the platform on which the simulator runs in real time, the analysis of the proposed methods is made from the perspective of implementing an automated process as well. Regarding the interpretation of the results obtained, the following observations can be made:

1. In terms of stability, the implicit methods are superior, being A-stable. The stability of the explicit methods is conditioned by the nature of the circuit (on which the eigenvalues of the resulting system depend) and by the value of the simulation step. If a circuit with the eigenvalues real part close to or equal to zero is simulated, it is necessary to use a method whose stability region includes the imaginary axis. Among the conditionally stable methods studied, the Predictor-Corrector (AB1-AM1) and Predictor-Corrector (AB2-AM2) method fall into this category.
2. Of the proposed methods, the only ones capable of correctly simulating an oscillating circuit are the AM2 and RK4 Gauss methods. The rest of the methods either show instability under these conditions or introduce an artificial attenuation factor.
3. Regarding the required resources and the minimum value of the simulation time step that can be obtained, the AM2 or RK4 (Gaussian) methods do not present

disadvantages compared to the AB1 or AB2 methods for the studied 2nd order system. The disadvantage of implicit methods is that, in some cases, they can transform a linear system into a non-linear one, which requires iterative solving methods that greatly increase the computational effort, the resources used and, finally, the simulation time step.

4. In terms of accuracy, the RK4 Gauss method proves to be the most precise. The major disadvantage of this method is the difficulty of modeling the real-time simulator. Using the RK methods can lead to the impossibility of transition from the representation in form of ODEs of the circuit to the representation in form of algebraic differential equations. This represents a problem for an automated real-time simulator generation system whose method of assembling the circuit's equations results in a system of algebraic differential equations (e.g. MNA method). The applicability of RK methods is thus restricted. On the other hand, the AM2 method has a comparable accuracy, being even easier to use.
5. In particular cases (which comprise the vast majority of switching sources), the implicit methods can be considered more efficient than the explicit ones from the perspective of both stability and accuracy. In order to obtain maximum generality, an iterative solution method of the resulting system may be required, case in which an explicit method with a stability region that also includes the imaginary axis (e.g. Predictor-Corrector method (AB2-AM2)) can provide better results. In this situation, the Predictor-Corrector methods prove their usefulness. However, for the particular system studied, the use of Predictor-Corrector methods results in a higher simulation time step and in an increased FPGA resource usage compared to the rest of the chosen methods.
6. Implementing real-time simulators on FPGA using Vivado HLS as a development environment allows obtaining simulation steps below 100ns for the Boost and PS converters. This performance allows the use of the AM1 method, providing a sufficiently high accuracy.
7. The correct modeling of limit cycling in a HIL simulation requires obtaining a simulation time step as small as possible. The real-time simulator inputs being sampled once at each simulation step, the resolution of the PWM generator "seen" by the simulator is reduced compared to the original one.

4.6. Conclusions

In conclusion, it can be stated that the methods chosen for the real-time simulation of the two stages of the EV on board battery charger led to a high degree of fidelity, a small simulation time step and a minimized number of resources used. The platform proposed for validating the converter model allows applying original methods for time and frequency domain characterization, allowing a comparative analysis between the physically implemented reference converter and its real-time simulator. The platform highlights the use cases of the real-time simulator both in HIL simulations and in error detection systems.

The Vivado HLS development environment lends itself to the development of real-time simulators, representing an optimal compromise between the level of abstraction used, the development time, flexibility, and the ability to control how FPGA primitives are used. The post-synthesis analysis tools offered by Vivado HLS prove to be particularly useful in quickly determining the simulation time step and in identifying the means by which it can be reduced.

5. Study 4 - Battery management and charging system integrated on a ZYNQ hybrid device

5.1. Introduction

The traction system along with the battery charging and battery management systems add, in the case of EVs, a number of additional functionalities to an electronic system already loaded with numerous sensors or auxiliary equipment designed to increase the comfort, safety and ease of handling. Considering this evolution, integration becomes necessary to reduce the size, decrease the cost and increase the reliability of the electronic system of the EV. The architecture proposed in this chapter exploits the parallelism and the number of digital resources of the ZYNQ hybrid device to implement the EV battery management and charging control systems on a single IC, demonstrating ZYNQ's capability to run in parallel a complex operating system (Linux), the logic required to manage complex communication protocols, the algorithms for estimating the state of charge and/or state of health, and the control methods of the power converters in the battery charger's structure.

Another aspect that the proposed architecture aims to improve is the replacement of the standard communication protocols used to transmit information between the elements of the battery management system with a protocol based on Wi-Fi technology. For the conventional implementation of the battery management system, the cell monitoring unit communicates with the higher levels of the system via the CAN or SPI interface, requiring galvanic insulation and a significant number of electrical connections (cables), elements that increase the susceptibility to errors caused by vibration or electromagnetic interference [28]. To overcome these shortcomings that contribute, among others, to the increase in cost and size of the product, one of the current trends is the migration towards wireless systems, proving that a battery management unit can communicate with thousands of sensors in a network inside a battery [28-29].

Among the functions of the battery management system, special attention was paid to the cell balancing method. In order to use the available energy in each cell with maximum efficiency, the conventional active balancing method based on the use of a bidirectional converter and an additional storage element has been replaced with the one described in [30], method capable of achieving efficiencies of up to 97%.

5.2. Working hypothesis / objectives

The objectives of the project described in this chapter are to implement a battery management system based on wireless communication and a battery charger control system integrated on the same device (ZYNQ). The ultimate goal of this approach is to increase the reliability, decrease the complexity of the required wiring and reduce the total number of ICs required for the implementation of battery management and charging systems.

Also, to improve the efficiency of the battery, an active cell balancing technique inspired from multi-level converters architecture is adopted.

5.3. Method

The block diagram of the proposed battery management and charging system is illustrated in Fig. 35. The EV on board battery charger uses the conventional two-stage structure (AC-DC and DC-DC stages) supplied from a single-phase grid connection. At structural level, the battery management system also borrows the conventional two-level architecture with a cell monitoring unit for each cell and a battery control unit designed to aggregate the data received from cell monitoring units, to estimate the state of charge and the state of health of the cells, to implement the various necessary protection methods, and to manage the balancing of the cells both during charging as well as during discharging intervals.

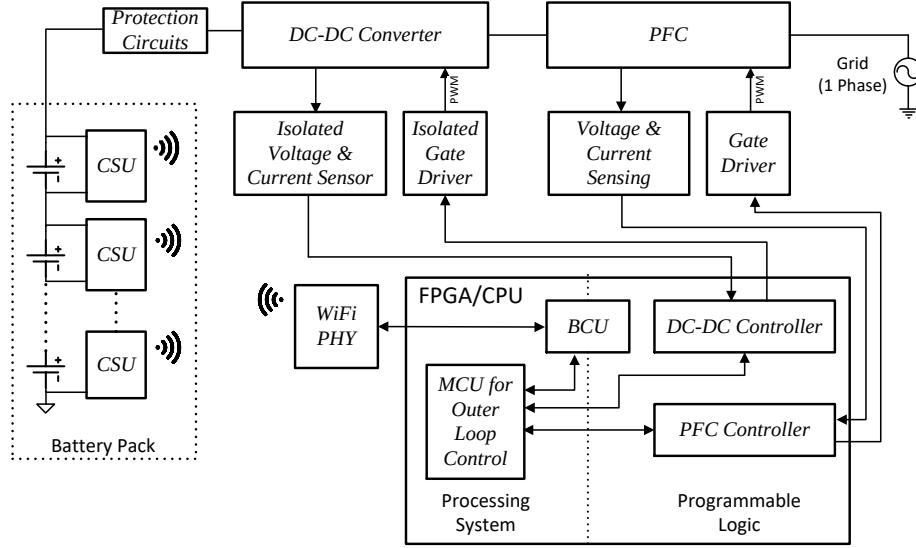


Fig. 35: Proposed charging and battery management system [20]

The main differences between the conventional and the proposed architecture are the use of wireless communication between the cell monitoring units and the battery control unit and the implementation of the later on the same device as the on-board charger control system [20]. The use of wireless communication confers the system a distributed nature at a lower level, which is in contrast to the effort and results of specialized integrated circuit manufacturers whose cell monitoring units manage a number of up to 16 cells [31]. Wireless communication can only be achieved using a distinct specialized device for each cell. To demonstrate the functionality of this concept, the standard Wi-Fi protocol and the TCP / IP stack were used. The complexity of these protocols is redundant for the given application and requires the use of a high-performance processor for the cell monitoring units. If battery management systems become attractive to industry, specialized integrated circuits, less complex and cheaper than those used for exemplification in this thesis, could be developed.

The integration of the battery control unit at the level of the ZYNQ device, in addition to reducing the number of controllers used in the system, also opens some interesting perspectives in terms of streamlining algorithms. Using the ZYNQ device, the tasks of the algorithms can be divided between the processing system and its programmable logic, greatly reducing the execution time of the algorithms. This is particularly relevant in the case of algorithms for estimating the state of charge and the state of health of the battery which, in order to obtain greater accuracy, may resort to the implementation of neural networks and fuzzy logic, requiring a resource-rich and high-performance digital platform [32].

The balancing method is based on providing each battery cell with a half-bridge. Upon discharge, the battery control unit identifies the cell with the minimum state of charge based on the data reported by the cell monitoring units and, by controlling its corresponding half-bridge, that cell is isolated until the next iteration of the balancing algorithm. This structure

similarly allows the cells to be balanced during charging, with the difference that, in this case, the cell with the highest state of charge will be isolated.

5.4. Results

For the experimental validation of the presented concepts a miniaturized setup was constructed. A COMEMSO battery emulator was used to emulate 4 distinct cells. To model a conventional battery pack the emulated cells are connected in series and to model the proposed smart battery pack the emulated cells are further provided with a half-bridge controlled by the cell monitoring units via Wi-Fi. The cell parameters are read by the battery management unit via the Wi-Fi interface also. In the proposed experiment, the load current is constant (2 A) and is controlled by a programmable current source.

The battery emulator measures the actual current flowing through the emulated cell and communicates the acquired value to the battery model running in real time on a PC in Simulink via a CAN interface. The CANoe program offered by Vector Informatik GmbH makes it possible to interface the COMEMSO battery emulator with the MATLAB environment. Based on the measured current, the real-time simulation model of the cell evaluates its state of charge and, next, based on a correspondence table between the state of charge and the no-load operating voltage of the cell, the voltage at its terminals is determined and emulated. To speed up the experiment, the capacity of the cells was reduced from 60 Ah to 1 Ah. The test setup used for the experimental validation is shown in Fig. 36.

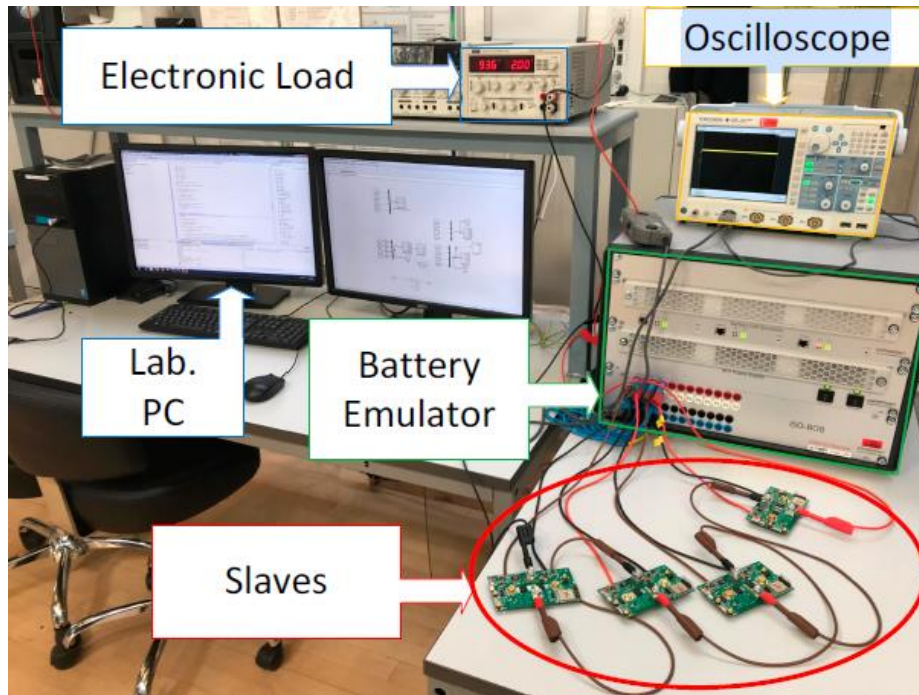


Fig. 36: The setup used for experimental validation of the proposed battery management system [33]

A first experiment is to determine the time required to balance the cells if a 5% variation in their state of charge is introduced. As seen in Fig. 37, balancing is achieved in about 300 s.

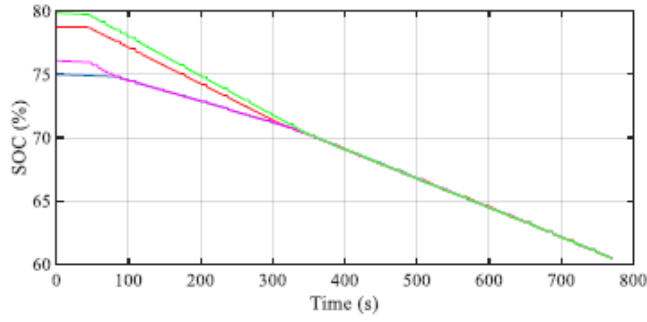


Fig. 37: Balancing function demonstrated using the battery emulator [33]

In a second experiment, designed to demonstrate the difference between the performances achieved with a passive balancing method and that achieved with the active balancing method used, a 5% variation of the cell capacity was introduced. Fig. 38 a) shows that a minimum state of charge of 25% for one of the cells is reached after about 15 minutes using a passive balancing method while applying the active balancing method the cells' state of charge remains equal during discharge, a state of charge of 25% being reached simultaneously by all 4 cells in about 20 minutes (Fig. 38 b).

To demonstrate the effects of a possible communication loss between the battery management unit and the cell monitoring units, the communication between the battery management unit and the cell monitoring units was deliberately interrupted after approximately 700 s of operation (Fig. 39). At this time, all cell monitoring units enter the SAFESTATE state, in which all cells are connected to the circuit. Entering this state also causes the rated voltage to increase (in an EV battery this increase represents a much smaller percentage of the rated output voltage due to the much higher number of cells). Fig. 39 a) shows the cells' state of charge from the perspective of the battery management unit. As long as the communication is interrupted, it remains constant, and when the communication is resumed (approximately 28 s after the interruption) it steps to its real value.

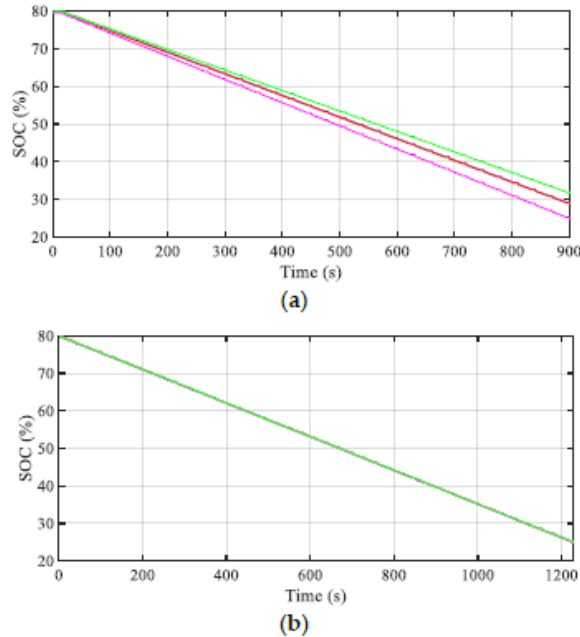


Fig. 38: The state of charge of the emulated cells when using a) a passive balancing method and b) the proposed active balancing method [33]

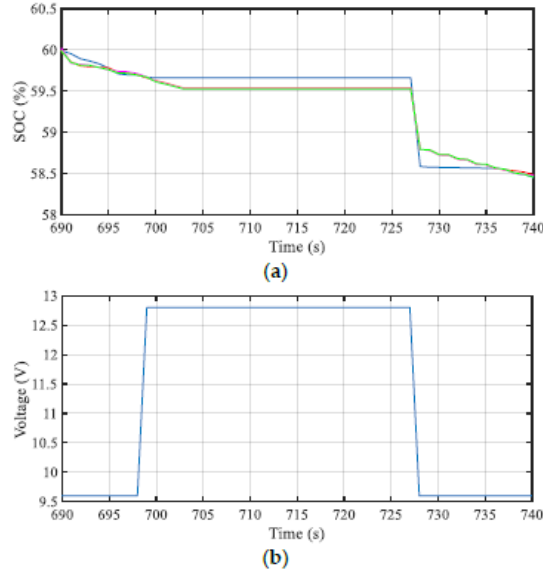


Fig. 39: a) the state of charge of the cells and b) the voltage at the battery output terminals during the interruption of wireless communication [33]

This step does not correspond to an actual step of the cells' state of charge, instead it represents the update of the values known by the battery management unit. One can observe that after resuming the communication between the battery management unit and the cell monitoring units, the balancing function operates within the expected parameters.

5.5. Discussions

The proposed battery management system only solves to some extent the problem of reducing the number of digital (smart) devices used. If the charger control system and battery management unit can be implemented on a single device, each cell will need a smart device to implement wireless communication. Obviously, the Wi-Fi protocol and the TCP / IP suite are not perfectly adequate for such applications. Using an operating system (which is required for easily managing the wireless communication) increases the processor load, requires additional memory and computing power which are otherwise not necessary. However, a protocol and a dedicated digital device for such applications could reduce the complexity and cost of the smart cell monitoring units. In addition to this (questionable) cost reduction, the use of wireless communication increases the scalability and reliability of the battery management system.

There are many advantages to using the ZYNQ hybrid device. First of all, the vast and high-performance resources of its programmable logic allow the integration of a large number of functions on a single device, allowing the proposed management and charging system to have an integrated nature at high-level. A second significant advantage is flexibility and scalability. The number of inputs and outputs as well as the performance of the dedicated arithmetic circuits cover the needs of the control system for a wide range of topologies used to implement the battery charger, ranging from conventional topologies to bidirectional multilevel converters. Last but not least, the hybrid nature of the ZYNQ device allows both the application of simple algorithms to determine the state of charge and state of health for the battery pack's cells as well as the use of algorithms based on Fuzzy logic and neural networks for increased accuracy. The complex set of embedded controllers that manage a wide range of standard communication protocols of the ZYNQ's processing system and the high-

performance ARM Cortex A9 processors that allow the use of a high-performance operating system provide the means for easily interfacing with other on-board electronic systems.

The differences between the conventional charging and battery management system architecture and the proposed architecture are summarized in Table 2.

Table 2: Comparison between conventional and proposed battery management and charging system [20]

Criterion of comparison	Conventional Architecture	Proposed Architecture
Distributed Control at battery cell level	No	Yes
Distributed Control at battery module level	Yes	No
Balancing efficiency	80-93%	>97%
Complexity	Lower	Higher
Scalability	Lower	Higher
Charger & BMS integration	No	Yes
Processing Power	Lower	Higher

6. Final conclusions

6.1. General conclusions

Based on the original architecture of the designed development platform and on the proposed methods, this thesis introduces a number of improvements to the development process of EV battery chargers. As HIL simulations are among the central elements of the proposed methods, the study of real-time simulation techniques of the charger stages has received special attention. The real-time simulation of switched mode power supplies with output power levels in the range of kW and switching frequencies in the range of kHz, a class of power converters used for the implementation of Level 1 and Level 2 EV battery chargers, proved to be an incompletely covered aspect in literature. Also, recently developed industrial software tools specialized in real-time simulation of electrical circuits prove to be insufficiently effective for the considered application. Thus, the main contribution brought by this thesis consists in filling this gap not yet covered by the research effort nor in industry or academia. In order to achieve the proposed results, the development effort was staged, the methods, personal contributions and partial results obtained being presented in 4 distinct studies.

Study 1 (Chapter 2) focuses on the mathematical modeling of the proposed converters for the design of the EV on-board battery charger. Following a detailed literature survey, the Boost converter was selected for the AC-DC stage of the charger and the PS converter for the DC-DC stage. Considering that one of the main goals of this thesis was to develop a real-time simulator for the charger, the main criterion for these choices was the degree of utilization of these topologies. Thus, most widely used topologies were chosen. For the AC-DC stage, the Boost converter is not the most efficient solution, but the real-time modeling of Interleaved Boost, Bridgless Boost or Totem Pole topologies (topologies for which superior efficiencies are reported) can be easily derived from the real-time simulator developed for the Boost converter.

For the DC-DC stage, the PS converter, due to its efficiency, ease of design, size and fixed switching frequency is one of the most popular topologies and is also used in renewable energy systems, smart grids or telecommunications equipment. The analysis performed for the two chosen topologies consist in mathematically modelling the steady state behavior, in

determining the averaged small signal model and the discrete small signal model. The models obtained were validated both by simulation means and (in the following chapters) experimentally and represent the basis for the design of the charger control system and the real-time simulator of the charger.

Study 2 (Chapter 3) deals with the characteristics of the control methods of the switched mode power supplies chosen as reference for the EV battery charger implementation. Both analog and digital control techniques were studied and an automated method of computing the control system coefficients was developed for both categories. Particular attention was paid to the time and amplitude quantization effects, inherent to AD conversion required by digital control methods. In this context, an original method for determining the static operating points in which limit cycling occurs was proposed.

In addition to these theoretical aspects, the FPGA implementation of the charger's control system was thoroughly analyzed. In this context, the sources of computational latency were explained in close relation to the specific primitives used by FPGA devices to implement arithmetic circuits. This analysis highlights the need to determine the influence of quantization errors of the compensator's coefficients on the accuracy and stability of the power converters in order to optimize the number of bits on which the coefficients are represented in order to obtain the lowest possible latency.

The lack of dedicated PWM generators in the structure of FPGA devices led to the development of an innovative architecture that ensures this function and maximizes the performance allowed by the parameters of these devices. Furthermore, a development platform that allows the experimental validation of the mathematical models derived in the previous study was proposed. Taking advantage of the flexibility of the FPGA device used, the proposed architecture allows open-loop or closed-loop operation of the system. With the help of a network analyzer, the possibility to insert a disturbance in the system was provided. In open-loop operation, the components of the loop can be isolated and their response in time and frequency domain can be determined experimentally. In closed-loop operation, the loop gain can be determined experimentally. This platform has a wide applicability and can be easily adapted for other converters or other control methods. The validation steps allow to greatly accelerate the digital control system development.

Study 2 also evaluates the benefits of using the Vivado HLS high-level synthesis program to develop the control system on FPGA. Following this evaluation, it was concluded that Vivado HLS offers a good compromise between flexibility, control of FPGA primitives, reliability, speed and ease of development. However, in some cases (the PWM generator for example), the means provided by conventional hardware description languages result in a more efficient use of the FPGA device and better performances. Referring strictly to the implementation of the compensator, Vivado HLS proves to be the optimal programming tool.

Study 3 (Chapter 4) presents a comprehensive analysis of real-time simulation techniques from the perspective of accuracy and stability properties. The proposed approach consists in a manual process of circuit modeling and implementation of the real-time simulator on FPGA. The modeling method is based on the representation of the circuit as a system of state space equations (equivalent to an ODE system), which are to be discretized using the AB, AM, RK and Predictor-Corrector methods. The evaluation of these methods was carried out on a 2nd order system (an RLC circuit). Specifically, the AB1, AB2, AM1, AM2, RK4 (in the Gauss form) methods as well as the Predictor-Corrector methods in the AB1-AM1, AB1-AM2 and AB2-AM2 combinations were considered. The real-time simulator of the RLC circuit based on these methods were simulated in Simulink and implemented using the Vivado HLS programming environment, leading to the following conclusions:

- Explicit AB methods are easier to implement but, due to their stability properties, they have limited applicability. Predictor-Corrector methods have stability properties superior to AB methods but, not being A-stable, they also have a limited applicability.
- The only methods capable of simulating an oscillating circuit are the RK4 Gauss and AM2 methods
- Using the proposed modeling techniques, the real-time simulators of the 2nd order system used as reference based on the AB1, AB2, AM1, AM2 and RK4 Gauss methods can be implemented using the same digital circuit, only the applied coefficients being different from one method to another. Thus, the simulation time step obtained for these methods is identical. Predictor-Corrector methods require a more complex circuit for the FPGA implementation. Consequently, a larger simulation time step is obtained for these methods.
- Predictor-Corrector methods do not bring additional benefits to AM methods in the particular cases studied. They can be useful in situations where the implicit methods convert a linear system into a nonlinear one. In such a case, Predictor-Corrector methods provide superior accuracy and stability properties compared to AB methods and do not require the application of an expensive iterative method such as the Newton Raphson method.

Based on these observations, the AM1 method was selected to implement the real-time simulator of the AC-DC and DC-DC stages. Due to the small simulation step obtained, even the accuracy of the 1st order methods proves to be sufficient. Because the converters used for the AC-DC and DC-DC stages of the charger have a finite damping factor, for the values of the chosen passive components even the use of the AB1 method leads to a stable system. The development platform presented in the previous study was improved by adding the real-time simulator of the PS converter for which the control system was developed. This created the prerequisites for running a signal level HIL simulation. The advantages of running these simulations include:

- The possibility to design, implement and experimentally validate the control system in the absence of the power converters. A research project focused on the development of innovative control methods can benefit from such a system, reducing the cost and saving the time required to develop and test the converter.
- Reducing the risk of damaging the power converter due to possible implementation errors.
- When designing an industrial product, the software system can be developed in parallel or in advance of the power converter, the development process being accelerated.

Highlighting the effects produced by the value of the real-time simulator's time step on modeling the closed-loop converter behavior is another original contribution of this study. Because the simulator inputs are sampled once for each time step, the actual resolution of the control PWM signal(s) "seen" by the simulator is altered. Because of this effective resolution loss, for the HIL simulation, the condition of limit cycling existence will be met, a phenomenon that will not occur when the control loop is closed through the reference converter. This false limit-cycle condition is also the reason why industrial real-time simulation programs cannot accurately model the behavior of closed-loop converters with switching frequencies of the range of kHz.

A second application of the developed real-time simulator can be found in the implementation of error detection systems. In such an application the "real" converter operates in parallel with the real-time simulator. The values of the converter's outputs (read by an ADC) are constantly compared with the outputs of the real-time simulator. In addition

to errors generated by component failure, aging defects of the components can also be detected allowing for timely intervention, thus increasing the reliability of the product.

The proposed development platform allows closing of the loop either through the real-time simulator (case in which a HIL simulation is performed) or through the "real" power converter, with the real-time simulator operating in parallel. The second configuration was used to illustrate the typical architecture of an error detection system, but also to perform a comparative analysis between the reference PS converter and its real-time simulator. The experimental results obtained prove the fidelity and usefulness of the developed model.

Study 4 (Chapter 5) presents an integrated implementation of the battery management system and the on-board battery charger control system. The main distinct properties of the proposed architecture are the wireless communication between the battery control unit and the cell sensing units and the implementation of an active method of cell balancing based on the addition of a half-bridge to each cell. These half-bridges are controlled by the cell sensing units, which in turn benefit from wireless communication with the battery control unit. The charger control system is the one presented in the previous studies and its validation was performed by means of the real-time simulation of the battery charger. The device on which the two systems were integrated is a ZYNQ hybrid device. The battery control unit operates mainly at processing system level, while the control blocks of the EV battery charger operate at the programmable logic level. The advantages of the proposed architecture are the reduction of the number of digital devices for the implementation of the high-level functions of the system, the elimination of wiring, the elimination of the external communication protocol between the charger and the battery management system, thus reducing complexity and the size of the EV on-board equipment and, finally, decreasing the costs.

Regarding further research, a first topic that may be further exploited is the transition from a system-level simulation based on a switched function models to a component-level simulation for the charger's real-time simulator. In this context, modeling the output capacitance and the drain-source resistance for the transistors of the resonant converters has a high utility. If the obtained simulation time step is small enough to model the resonant effects (with characteristic frequencies in the range of tens of MHz) corresponding to switching events, the real-time simulation model can allow the detection of hard switching and also performing an efficiency estimation. This experiment is likely to require a state-of-the-art FPGA device.

Another aspect that can be more thoroughly elaborated is the implementation of error detection systems. The thesis briefly stated and illustrated this scenario of using real-time simulators. The reasons for failure of power converters, the aging effects of components and the means of determining them require further studies.

6.2. Originality and innovative contributions of the thesis

The originality elements of this thesis are:

1. The architecture of the proposed system that facilitates and accelerates the process of developing the digital control system of the EV battery charger.
2. The manner in which the AD and DA interfaces are used to experimentally determine the frequency response of power converters (or their real-time simulators) when the control loop is open and the loop gain when the loop is closed.
3. The discrete PWM generator architecture that maximizes the performance that can be obtained on FPGA devices.

4. The comparative analysis of the methods that can be employed to numerically solve ODE systems from the perspective of implementing real-time simulators of electrical circuits.
5. The development of a real-time simulator based on a switched function model for the PS topology.
6. The low value (20ns on a ZYNQ XC7Z020 device) of the simulation time step obtained for the real-time simulators of the Boost and PS converters.
7. The portability, fidelity, simplicity and the small amount of digital resources required for the real-time simulators implementation.
8. The study of the impact that the time step has on the ability to model limit cycling.
9. The ability of the developed platform to exemplify the use of the real-time simulator developed both in HIL simulations and in error detection systems.
10. The use of low-cost development boards and tools for applications that are conventionally implemented on much higher-cost platforms.

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