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Electronics, Telecommunications and Information Technology

PhD THESIS
– ABSTRACT –

Research on High-Performance Power Electronic Traction Transformers for the Novel Medium-Voltage DC Railway Electrification System

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Introduction and motivation

In the second half of the last century, the use of individual transportation went through a rise, because trucks, cars and airplanes became more popular choices than public or industrial transport, due to their speed. This resulted in the decay of the railway network. However, this rise lead to congestion of the public transfer system by the end of the century and railway transit became again appealing.

During the 20th century, the power electronic industry also went through major growth and many innovations were implemented. The railway electrification system was developed, which is an external power supply exchanging the on-board fuel supply in trains or trams. Electric power is generated in large power plants and is transmitted to railway feeding stations, which then supply the trains via the railway network. Few electric railways have their own generating stations and transmission lines; therefore, the railway electrification system relies on the electric utility grid to supply their stations. Between the stations, railway has its own transformers, distribution lines and switches. The moving trains receive the power from conductor lines running along the tracks. These conductors can be either overhead suspended lines or third rails mounted at track level, while the return conductor in both cases is the running rail. Fig. 1 illustrates a typical railway electrification network and the various rolling stock types.
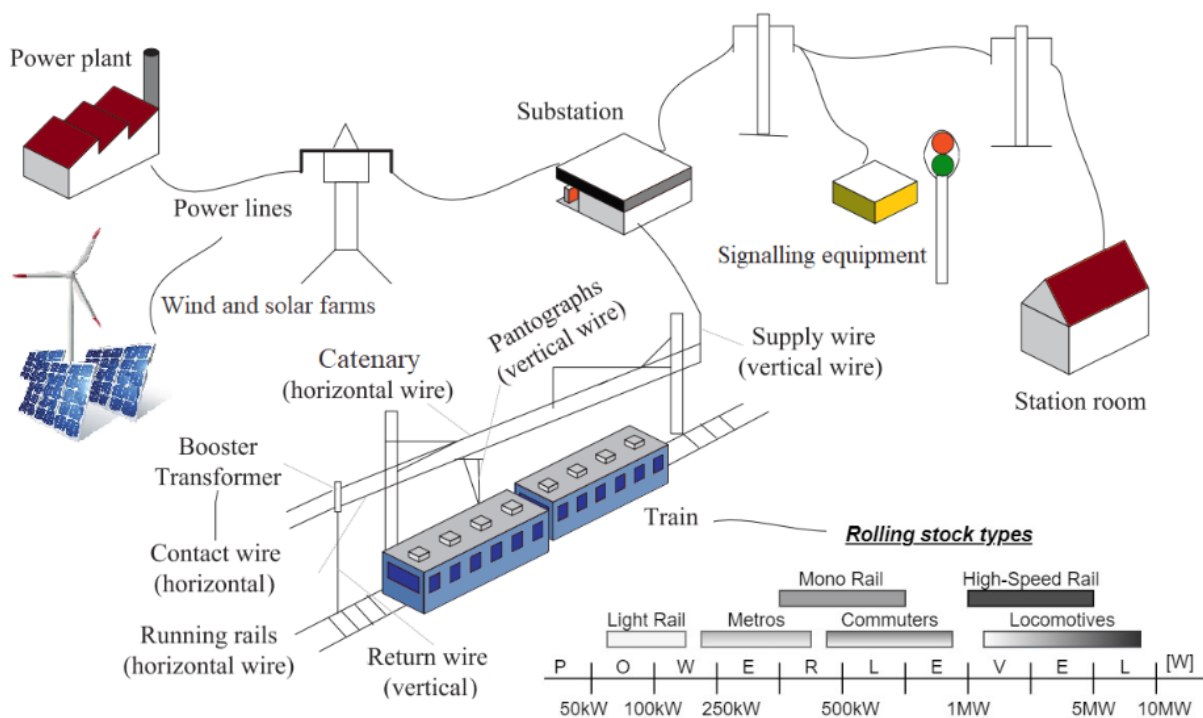

Fig. 1 – Typical railway electrification network and the different rolling stock power levels.

The European railway electrification system, on the other hand, was not really modernized and the standard 25kV AC and 15kV AC lines are used, with a few exceptions of some low-voltage DC lines. The issues are their continuous dependence on the utility grid and the lack of significant improvement in the railway electrification network. During the last decades, renewables grew a lot, and Europe's tendencies on emission reduction and renewable integration also changed. While distribution grids, micro-grids, and other smart grids have been developed to facilitate the new trends, the railway network still hasn't been integrated into the new vision and roadmap. The currently working traditional railway electrification standards are shown in Table 1:

Table 1 – Railway electrification standards [1]–[4].

Railway Electrification system	Voltage				
	Min. non-permanent	*Min. permanent*	*Nominal*	*Max. permanent*	*Max. non-permanent*
600V DC	400 V	400 V	600 V	720 V	800 V
750V DC	500 V	500 V	750 V	900 V	1000 V
1500V DC	1000 V	1000 V	1500 V	1800 V	1950 V
3kV DC	2 kV	2 kV	3 kV	3.6 kV	3.9 kV
15kV AC, 16.7Hz	11 kV	12 kV	15 kV	17.25 kV	18 kV
25kV AC, 50Hz (EN50163) and 60Hz (IEC60850)	17.5 kV	19 kV	25 kV	27.5 kV	29 kV

Railway electrification utilizes AC single-phase power, which requires connection to high-voltage transmission lines that are not always available in the locations intended for railway feeder stations and frequently necessitates complex and extremely costly modifications to existing layouts, such as tap and looped connections at the substations. Additionally, transmission operators do not view new electric railways favorably because they introduce intermittent load peaks that compromise system stability, particularly in future scenarios where the power system's inertia is significantly reduced due to widespread adoption of renewable energy sources. With the advancement of technology and the availability of high-voltage semiconductors [5], it became possible to employ higher and more efficient DC voltages previously only possible with AC [1], [6]. This enables the development of novel concepts. Several new projects and proposals are dealing with the integration of renewables into different grids and networks and also with the integration of the latest electrical technology by creating innovative power electronics circuits and equipment. This thesis is based on a novel European Union H2020 project called Flexible Medium Voltage DC Electronic Railway System, which explores the con-cept of a smart, interoperable medium voltage railway grid, compatible with renewables and capable of supporting the utility grid. At the same time this project was being developed, other similar projects and proposals were being conducted throughout the world [5], [7], [8]. This project was the one that suggested a 25 kV DC voltage for the catenary lines since new materials and semiconductors make it possible to make DC circuit breakers for this level of voltage. The work in this project was shared between the Technical University of Cluj-Napoca and the University of Birmingham, with one PhD student from each. This work covers the Power Electronic Traction Transformer on the locomotive, which is the second work package of the project.

Currently, the electronic traction equipment is a large and heavy transformer system with a line frequency transformer as galvanic separation. In the case of traditional 25 kV AC systems in Europe, it is a 50 Hz transformer, while in the case of 15 kV AC systems, it is a 16.67 Hz transformer. With such systems, the power density of on-board traction systems is very limited. Moreover, to accomplish this goal of improved integration of renewable energy sources and energy storage, there is currently a need to develop viable and less expensive alternatives to existing electrification systems that do not rely on high-voltage transmission lines. Typically, heavy or high-speed railways have a power range of 100-500 MVA with 50-100 MVA peak power for individual supply, which is compatible with the capacity of common medium-voltage distribution systems. The connection of railway feeder stations to the power distribution network, on the other hand, would be conceivable only if no system imbalances were introduced. DC power supply meet this criteria since the DC volt-age is created by three-phase diode rectifiers that draw balanced current with a high power factor. On the other hand, because of constraints on the highest short-circuit breaking current, the DC voltage level is limited to roughly 3 kV, hence limiting the railway's maximum power output.

Additionally, a higher voltage power supply would create issues for the trains' traction system, which operates at voltages of a few kV. As a result, the old notion of direct current railways does not mesh well with the future vision of an electric railway that is more integrated with the power distribution networks, as the diode rectifiers are unidirectional, preventing any control of power flows with the grid. Since a new medium voltage DC line is being proposed in this project, the most advanced currently proposed modular systems need to be adapted to work with the new 25 kV DC catenaries.

Hypotheses and Project Concept

The MVDC-ERS concept envisions a new type of medium voltage direct current (MVDC) traction power supply based on controlled bidirectional converters to enhance the railway's grid connectivity. This will not only increase railway supply efficiency, but will also add capacity to the power distribution grid, as railway electrification lines can be utilized to expand capacity between the nodes where the substations are connected. This is especially critical in future scenarios where a greater proportion of renewable energy sources is integrated into the power system and control of power flows is vital for ensuring the power system's proper operation. The proposed new MVDC railway system incorporates significant new concepts for both railway power supply and train propulsion systems. Multilevel medium-voltage power converters may give a solution to the technical issues associated with MVDC rail power supplies. These converters are built of individual building blocks working between 3.3 and 6.5 kV that can be connected in series to achieve the necessary DC voltage level. However, there are still a number of issues that need to be addressed before the design can be considered adequate. These include the efficiency of the power converters, an analysis of the cost of connection in comparison to traditional single-phase AC feeder stations, interference with signalling equipment due to the presence of high-order harmonics introduced by the converter, the integration of renewable energy sources and network protection, the design of compact power electronics-based DC transformers for locomotives, and the integration of on-board energy storage to enable discontinuous electrification.

The provision of the network with static converters creates entirely new possibilities for interfacing with the power grid, which is critical given the increased penetration of renewable energy sources. Likewise, feeder stations can be used to feed the railway in a mesh configuration, and these can be managed to optimize both the railway and the power grid's operations. Fig. 2 illustrates an example of a segment of railway that is fed by two supply stations with on-site renewable energy sources. Depending on different traffic conditions, the rail-roads can be operated a) to mitigate heavy traction loads with renewable energy sources, b) to reduce grid power consumption when the railway has light loads, c) to maximize regenerative braking energy recovery, and, most importantly, d) to support distant nodes of the power distribution grid by using the electrification line as a parallel path, thereby increasing the power system's capacity.

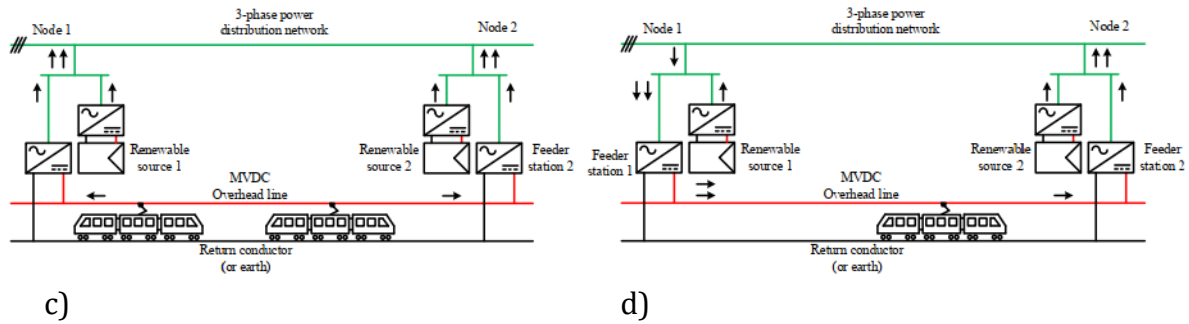a)   b)
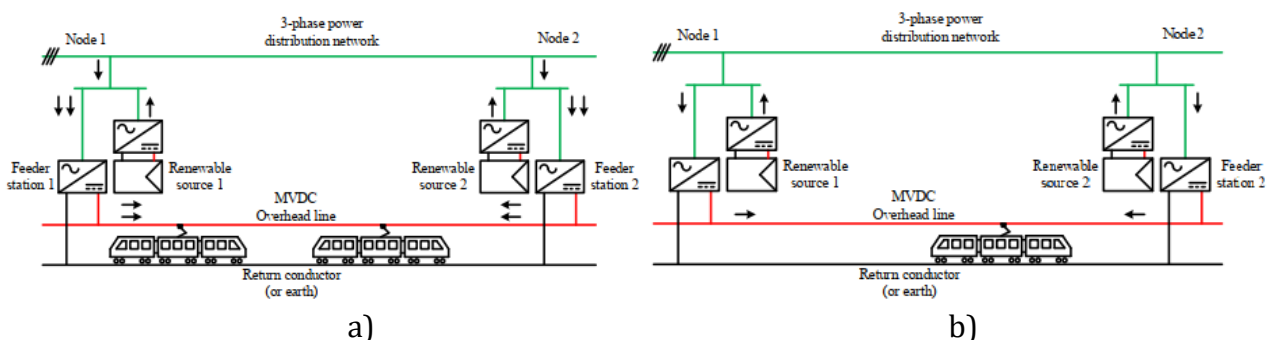
Fig. 2 – Operations mode of the MVDC railway: a) high traction load; b) low traction load; c) regenerative mode; and d) grid support mode.

In terms of on-board traction systems, the primary issue with MVDC electrification is the need to develop viable alternatives to transformers for stepping down the voltage to levels compatible with traction inverters and motors. Single-phase PETTs, also known as solid-state traction transformers, are a MV high-power-density converter technology that replaces line-frequency traction transformers with a combination of power semiconductors and medium-frequency trans-formers for on-board electric traction applications. While we are aware that some work has been done on PETTs previously – most notably in the ASEA Brown Boveri (ABB) project –, such work was largely based around AC transformers using Power Electronics, whereas our research is focused on DC-based power transformers. Various types of innovative converters will be investigated for use in MVDC traction applications.
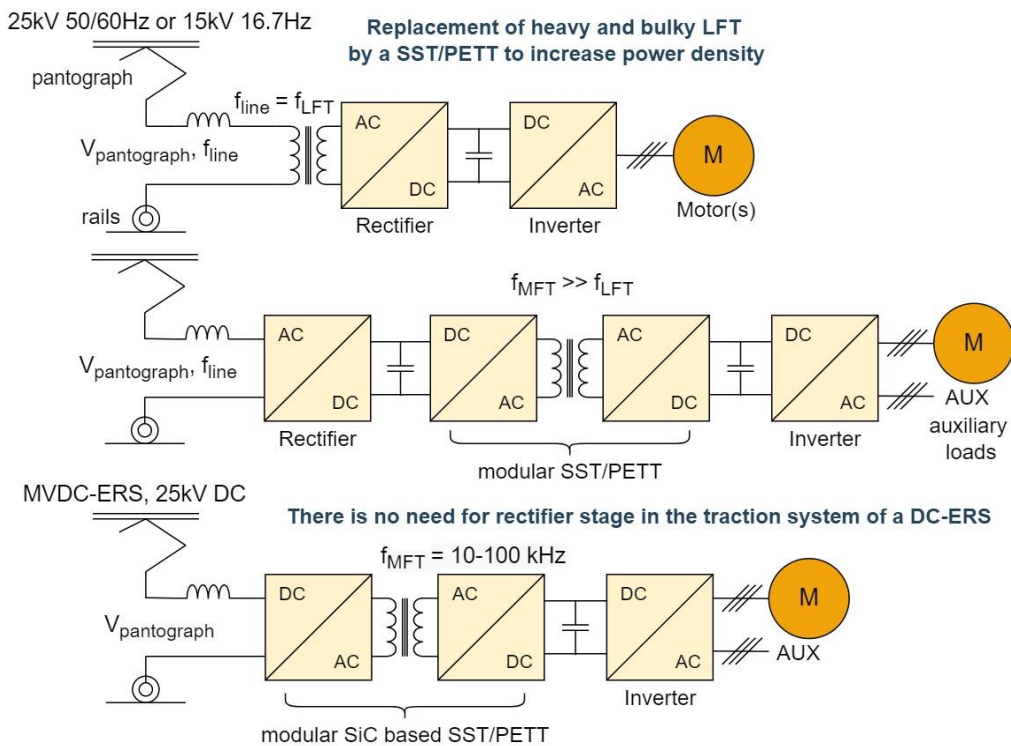

Fig. 3 – PETT replacing traditional line frequency transformers (LFTs).

The introduction and state of the art sections of the thesis (Chapter 1) includes a detailed comparison of the novel MVDC-ERS concept with the traditional railway electrification lines (chapter 1.3) and it traces back to the origins the idea and tehnology of PETTs and then follows their developement until the modern day modular topologies, concluding with Table 2 – comparison of the this new tehnology with the traditional line frequency transformer based systems (chapter 1.4). Finally, this large introductory section of the thesis includes a detailed study on regenerative braking, on-board storage and the potential benefits of using wide band-gap semiconductors in MVDC converters (chapters 1.5 and 1.6). It must be mentioned, when

addressing high voltage semiconductors, that the resistance of the ideal drift region can be correlated with the fundamental properties of the semiconductor material. According to [9], the specific resistance of the ideal drift region can be calculated as follows:

$$R_{on-ideal} = \frac{4BV^2}{\varepsilon_S \mu_n E_C{}^3}$$

(1)

In (1) the denominator is referred to as „Baliga's figure of merit for power devices" and indicates the impact of material properties on the resistance of the drift region of a semiconductor. The cubic dependence on E_C – the critical electric field for breakdown of the on-resistance, favors WBG semiconductors such as silicon carbide, but the dependence of this resistance on the square of the breakdown voltage would affect semiconductor losses if too high voltage SiC devices are selected for an application. Due to the on-resistance being directly proportional to BV^2, two 6.5kV SiC devices in series would be more efficient than a single 10kV or 15kV SiC device in terms of power losses (since P is proportional with R). Therefore, in an application such as MVDC-ERS, the choice of semiconductor voltage will likely be determined by cost and power density gain. A reasonable choice must be made between these and the efficiency of the converter.

Table 2 – MFT and LFT technology comparison.

	LFT	MFT
Power density	low	high
Efficiency	limited and lower	high
Transformer design complexity	low	high, moreover different applications need different and specific design
Operating/switching frequency	line frequency (low)	hundreds of Hz to tens of kHz
Power quality	fair	good, due to more control options
Technical maturity	reached its maturity	not yet mature, some topologies and configurations are reaching their potential faster than others
Fault current limitation	low	good
Fault isolation capability	poor	good, also redundant configuration is available
Control complexity	low	high and in some applications can be difficult, but rewarding
Switch and drives count	low	high number of devices, due to modular/multi-level structure, however WBG high-voltage devices can lower it
Flexibility	low	high, offers additional functionalities like fault limitation and isolation, voltage flicker compensation
Controllability	low, no control over transmitted power	high, good control over power flow
Availability	high	fair, difficult to design and manufacture
Reliability	high	lower; under research and development, different configurations, like redundancy can bring improvements
Costs	low cost compared to state of the art technologies, much better kW/cost value	due to multilevel/multi-stage and/or multi-modular structure they have a higher cost (still low kW/cost value)
Losses	higher losses	lower losses

Objectives, Project Stages and Methodology

The part of work from the project designated to the PhD student from the TUCN, myself, has the following objectives:

- A technical literature overview and study on topologies of static converters for the medium voltage DC transformers for railway traction;
- Study on SiC semiconductor technology and their efficiency in DC traction applications;
- Comparison and critical analysis of the MVDC railway traction transformer topologies and configurations;
- Definition of the optimal topology for application to railway traction and evaluation of the performance of the converter;
- Development of a mathematical and software (simulation) models for the prediction of static and dynamic performance of the DC transformer, also addressing the control requirements of the converter and protection issues;
- Implementation of a small-scale prototype of the DC-DC transformer.

The working principles and methodology used to reach the objectives proposed previously and the related project stages are:

1. Documentation and choice of research direction

As a first stage in order to elaborate the project proposed, it is necessary to analyze and synthetize a large number of relevant works in the field. Besides the well-recognized works that describe aspects related to the modeling and design of basic topologies, it is important to keep an eye on the publications with high impact in order to be able to account for the novelties appeared due to the great interest shown in new SiC semiconductor devices for power electronics. The titles considered will be listed in the reference section of the PhD project. This process will take place throughout the elaboration of this work and depending on the evolution of the domain, proposed structures as well as direction of research can be changed to obtain significant novelty elements.

2. Modeling

Once the topologies to be studied are chosen, their mathematical modeling is required. For the design and performance evaluation of a converter suitable for railway traction, regardless the topology, it is required a steady state analysis and deduction of small signal model – for the control loop to be designed. For mathematical modeling can be used some dedicated software like Mathcad and Matlab to simplify the process, while the software models will rely on PSIM with fixed step solve and later on Matlab/Simulink, where basic power electronics blocks can build the system, including control algorithms. Having a mathematical model, simulation and experimental results, a comparison will be obtained. The results have to coincide before going on to the next development stage. Modeling is important regarding the definition of requirements for control, passive and semiconductor elements ratings.

3. Implementation

All chosen topologies will be composed of a control circuit and a power electronics circuit allowing a modular implementation at hardware. A prototype will be realized of a module of the DC railway PETT. Before choosing, different types of controllers will be evaluated based on microcontrollers, digital signal processor or field programmable gate array. The implementation of analog control has limited flexibility due to integrated circuit components with fixed functionality. Manufacturers like On Semiconductors, Infineon, Texas Instruments, etc. offer solutions for all topologies. However, for topologies that have not yet been adopted by the industry, the easiest solution is to use digital control. Not all proposed topologies will be implemented, only those with promising results following mathematical modeling and simulation.

4. Experimental validation

To advance to the last stage, the new DC electrification system will be tested in Power Electronics Laboratory at UoB and TUCN. In the validation process, for the implemented topologies it will be necessary some measurements of specific parameters such as DC values, voltage and current ripples at the output of the converters, duty cycle, the system response at a load step and power losses. The results and measurements of these parameters will be compared with those obtained in mathematical calculations and in the simulation model. The difference between the obtained experimental values and simulation should not exceed 10%.

Literature Research and Results

This study covers the first major stage of the project and it will undertake a comparative evaluation of topologies of static converters for the medium voltage DC transformers. In addition, it will define the optimal topology for application to railway traction and evaluation of the performance of the converter. As part of the literature research, a study on the type of semiconductor devices was already carried out in chapter 1.6 of the thesis, to quantify the typical efficiency levels in comparison with traditional transformer, including the possibility of using SiC and other emerging WBG devices. Therefore, this chapter focuses on the detailed literature review of existing topologies of converters for use as DC transformers in this project and the choise of the optimal topology to be implemented. Two such converter topologies will be proposed at the end of this chapter, as candidates for the PETT modules. The final definition of the topology, will lead to the definition of the requirements of the control.
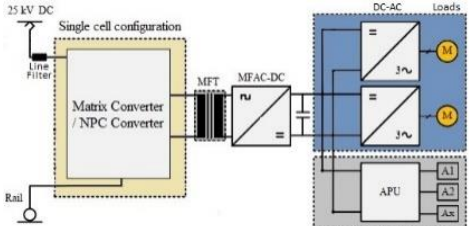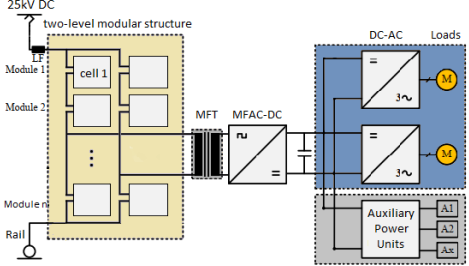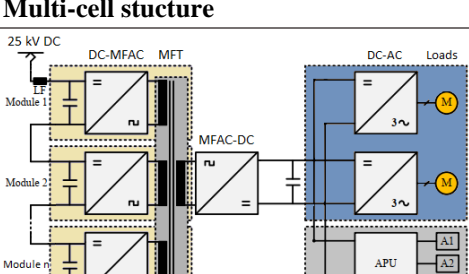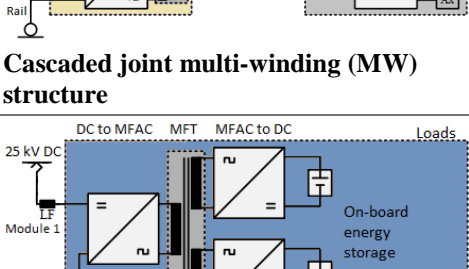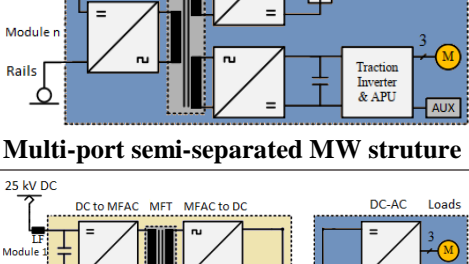
This chapter traces the reader through the evolution of modern PETTs and what has been achieved in the last 25 years. The most popular industrial trends will be presented and the analysis and comparison of different aspects will be summarized in tables and figures.

Power Electronic Traction Transformers

Various university research groups and train manufacturers have examined, designed, prototyped, and tested a number of PETT topologies for railway systems based on the early concepts presented in the introductory chapter of the thesis [10], [11]. The new WBG semiconductor materials, such as SiC, support the development of PETT, particularly when the 6.5kV and 10kV SiC components are commercially available. SiC semiconductors enable switching frequencies as high as tens of kilohertz, which increases the fundamental frequency of MFTs; when SiC devices are available for higher voltages, it will be possible to employ fewer converter modules and/or stages. The operating frequency of modern PETT architectures is almost identical to the switching frequency of power semiconductor modules, and is therefore independent of the line frequency. The immediate application of PETTs would be for 15kV AC ERS-connected traction vehicles, as the 16.7Hz supply frequency requires locomotives to have bulkier on-board transformers than for 25kV, 50Hz or 60Hz AC systems. In this scenario, the new PETT system achieves a 7% increase in efficiency and a 50% reduction in global weight [1]. A new ERS, such as a flexible MVDC-ERS, would require novel high-performance PETT structures to address new challenges, including fault handling, protection circuits, and smart-grid compatibility. In MVDC-ERS traction topologies, the rectifier stage is unnecessary because the line voltage is DC.

Table 3 provides a brief review and comparison of the most important PETT configurations analysed in this chapter. In addition, Fig. 4 presents a classification tree of traction transformers based on the present study, which aids in tracing the growth and expansion of PETT technology.

Table 3 – State of the art topological families – summary and comparison.

Topology	Applications	Advantages/ disadvantages
Single cell SST structure	Developed in '85 by Weiss with matrix converter and 400Hz MFT. Later the concept was further studied and the newly available IGBTs of high voltage were employed. Currently applicable to LV systems.	+ higher switching frequency, lower losses, less modules and costs + future potential, when 10-15 kV SiC transistors will appear − design for reliability is challenging (redundancy) or increases complexity
Multi-cell stucture	In 2001 researches demonstrated the necessity of series connection of converters in the front end. Right after in 2002 the multicell concept was presented. Now there are some cascaded (modules) multi-cell topologies also.	+ scalable to higher voltages and reliable (redundant cells) + dynamic voltage sharing capability − control can be more difficult − many stages and levels increases costs +/- only one MFT
Cascaded joint multi-winding (MW) structure	Currently the most commonly used converter configuration is the ISOP. In 2003 Alstom developed a converter with semi-separated multi-winding transformer. Usable for EMU setup with independent output DC links in secondary.	+ power distribution balanced between modules + mature and popular + modular design, fully controllable − joint multi-winding MFT is difficult to make and has weaker fault-handling capability − ISOP: complex control
Multi-port semi-separated MW struture	In 2014 a similar configuration as the previous was developed in China, but with multi-port configuration in the secondary as a novelty. Usable in 25kV ERSs.	+ voltage balancing control achievable, more ports available − joint multi-winding MFT is difficult to make and has weaker fault-handling capability
Cascaded ISOP with separated MW structure	Currently the most preferred topological family. Since 25kV is a higher voltage by 66% than 15kV, it implies more cascaded modules and higher costs, when applied to a 25kV ERS.	+ whole system ISOP structure, fully controllable and with improved reliability due to separated windings + most popular and mature + transformer less difficult to produce and has better fault handling capability − high number of power devices, higher costs

Regarding ISOP configuration, for the DC-DC stage various different topologies can be used. The most promising and useful topologies would include LLCs, Phase-Shift Converters, DABs or even multi-cell modules. As the review in this chapter reveals, CHB configurations are more mature and can reach higher voltages than other multilevel topologies, including diode-clamped configurations.
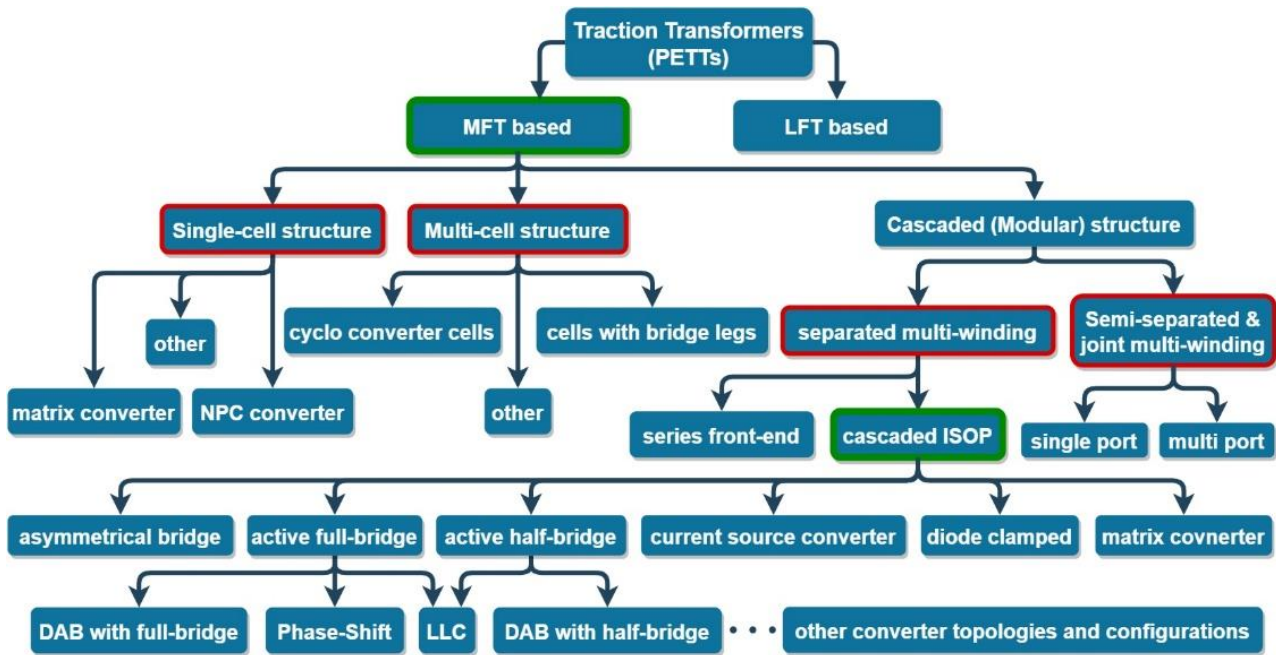
Fig. 4 – Summary of the classification of PETT topologies.

Conclusions and Discussion

Due to the large number of high-voltage power devices and advanced cores used in MFTs, PET-based systems are more expensive than standard LFT-based systems, although they offer a number of attractive advantages. First, the enhanced efficiency and power quality, next a redundant design that increases availability, and last, the higher power density. In other instances, however, the large number of components limits their reliability and necessitates a more complex design and control procedure. LFT-based systems are not even an option for MVDC traction, as the requirement for two converters and the flexibility to choose the intermediate AC frequency will inevitably lead to MFTs for the greater attainable power density.

Regarding the discussed pros and cons of PET-based systems, it is essential to note that the benefits are readily apparent, whereas the majority of disadvantages are reliant on technologies and materials. Further development of power devices and materials, as well as research into topologies and control systems, is likely to mitigate the majority of the disadvantages.

MVDC-ERS describes a new DC railway electrification system based on the new technology that makes its implementation possible. This innovative approach will provide new opportunities and features for an interoperable smart DC grid. Simultaneously, the new system will integrate the benefits of modern technologies with those of existing ERSs. Additionally, the onboard PETTs will need to be redefined for the new system and its requirements.

The literature research of converter topologies concluded that the optimal PETT topological family for the MVDC railway concept is the cascaded modular ISOP configuration with separated multi-winding (SMW) isolation, the fifth in Table 3 [12]–[14]. The Active Full-Bridge converter topology was recommended as a sub-topology for the modules; hence, two active-bridge converters will be modeled, built, and implemented in the following chapter as candidates for the traction transformer of this project. Fig. 5 depicts the final specification of the topology.
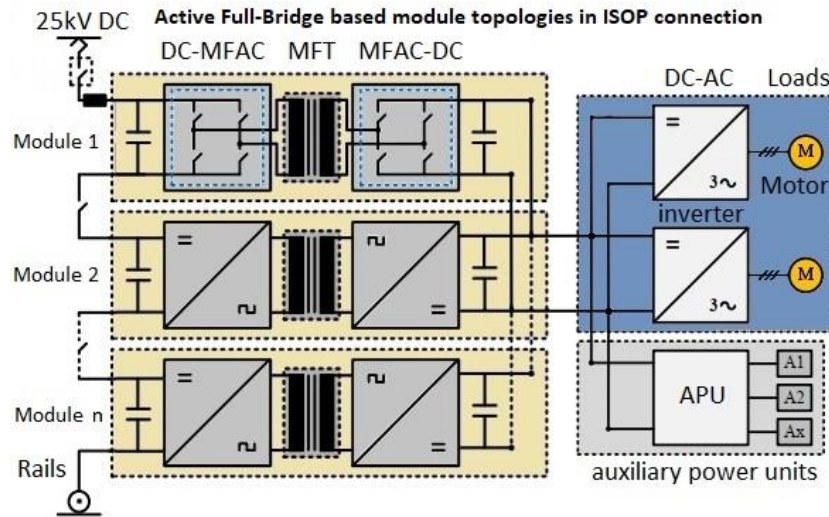
Fig. 5 – Cascaded modular ISOP connected active full-bridge converters.

Full bridge DC-DC converter utilizes the power switch on both the upper and lower bridge arms. These switches maintain the consistency of the bridge arm's on-off, making it simple to eliminate the bias issue and achieve soft-switching mode. And because the working current is double that of the half-bridge converter, full-bridge DC-DC converters are typically employed in high power supplies. Currently, bidirectional DC-DC converters are frequently employed in high-power applications. These can be controlled by "phase-shifted" signals, which can exploit the parasitic inductance and stray capacitance of IGBTs/MOSFETs to accomplish ZVS of the switches, minimize switching losses, and increase switching frequency. As a closed-loop control system, it must regulate the on-off time of the converter's switches to maintain output stability and obtain satisfactory static and dynamic characteristics through the use of feedback from the closed loop.

Modelling and Implementation

This chapter covers the second major stage of the project and it will present the development of the matemathical models for the medium voltage DC transformers. In the previous chapter, the optimal topology for application to railway traction was defined. It was found, that the active full-bridge based cascaded modular PETT topology should be the suitable candidate for this project. Therefore, two converter topologies will be developed and implemented in this and the following chapter. This section focuses on the detailed matemathical model of the Dual Active Bridge and Bidirectional Phase-Shift Full-Bridge converters and on the design of their compensator loops. Converter modules in ISOP connection can be controlled coupled or decoupled. This chapter will discuss the mathematical model of the ISOP connection, for the DAB converter and will present the decoupled control mode as well. Furthermore, three differend snubber circuits will be presented and compared along with their design procedure. In this chapter the converter models and design sheet will be developed as tools for the full-scale and experimental simulations from the next stage.

Dual Active Bridge Converter

The DAB converter is a DC-DC converter implemented by a rectifier, a high-frequency transformer and an inverter. This PETT topology uses WBG power devices, such as silicon carbide (SiC) and it is expected that such a PETT technology can be operated at higher, fixed frequency, can have less cascaded modules and power devices, can withstand higher voltage of the electrification system, and can be smaller.

The Dual Active Bridge converter is a topology with fewer components, soft-switching commutation, low cost, and high efficiency. This topology is applicable where power density, affordability, weight, and reliability are crucial. The topology is shown on Fig. 6. Some advantages of DAB converters:

- It can be bidirectional

- Compatible with MFTs

- Configured with small duty cycle values (output current closer to linear)

- It can be controlled via phase-shift, duty cycle, or both (single-phase-shift, dual-phase-shift, extended-phase-shift, triple-phase-shift)
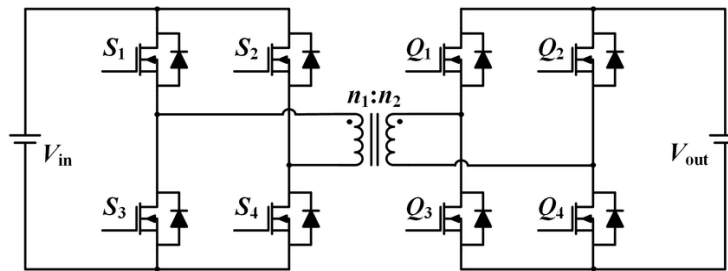
Fig. 6 – Dual active bridge converter.
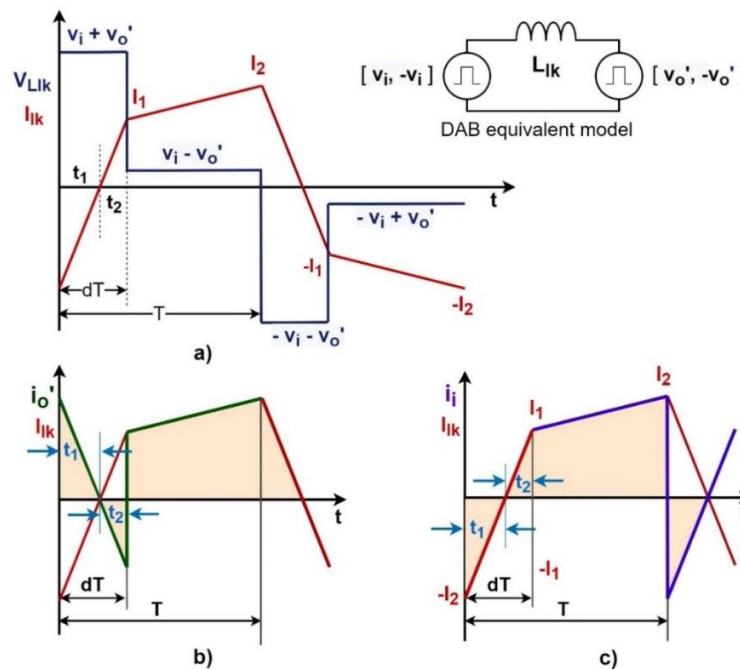
Fig. 7 – Dual Active Bridge converter - waveforms: a) presents the leakage inductor voltage and current more detailed, b) shows the output current reflected in the primary, compared to the leakage inductor current, and c) represents the input current in the same manner.

As shown in Fig. 7, for the time interval between 0 and d·T (d being the duty cycle and T being half of the switching period), the voltage on the leakage inductor is equal to the sum of the input voltage – denoted v_i, and the output voltage reflected in the primary – denoted v_o' ($v_o' = v_o/n$, where n is the transformer turn ratio). Similarly, for the time interval between d·T and T the voltage on the inductor is $v_i - v_o'$. Starting from these waveforms, in the thesis the complete mathematical model was deduced, including the avarage (Fig. 8) and small signal models. Peak values, voltage transfer ratio and finally the transfer function – presented here in equation (2) – were also obtained.
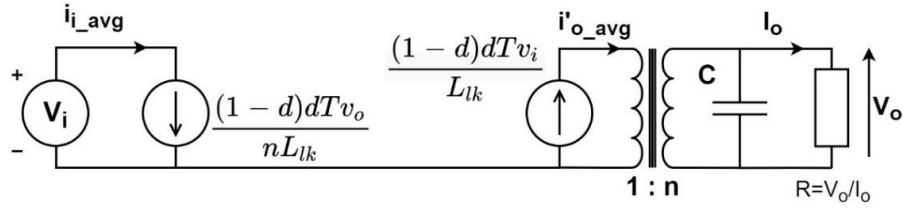
Fig. 8 – Average model of a DAB module.

$$H_{DABo}(s) = \frac{\widehat{v_o}}{\widehat{d}} = \frac{v_i TR(1-2d)}{(RCs+1)2nL_{lk}} = \frac{v_o(1-2d)}{(1-d)d(RCs+1)} \tag{2}$$

As observed on Fig. 8, the avarage input and output currents are:

$$i_{i_{avg}} = \frac{(1-d)dTv_o}{nL_{lk}}$$
$$i_{o'_{avg}} = \frac{(1-d)dTv_i}{L_{lk}} \tag{3}$$

A design sheet was implemented in Mathcad with the converter equations to calculate the component values and to obtain the controler parameters based on the transfer function. Having a first order transfer function, a PI compensator was designed to control the output voltage. The PI design process is automatized in Mathcad. A screenshot from the Mathcad design sheet is presented in Fig. 9 (the phase margin is 70 degrees and the cutoff frequency is tenth of the switching frequency).

Fig. 9 – PI design equations in Mathcad.

To verify this design procedure, the compensated loop's transfer function, $H_c(s) = H_{DAB}(s) \cdot H_{PI}(s)$, is plotted in Mathcad.

Converter Modules in ISOP Connection

Connecting power converters in an ISOP configuration is a common way of increasing power transmission and power density. Using the same converters in each module streamlines their interconnection, although imperfections, parasitic, and other errors might cause input voltage balance issues. To examine this problem and its solution, a four-module power system, as depicted in Fig. 10, is explored. The duty cycle of the converter bridges is fixed at 50%, and the phase shift between the primary and secondary side bridges is the control variable. For the input and output current equation (3) is used to explain the average behavior of the converter, where d is the control variable, T is half the switching period, n is the turns ratio and L_{lk} is the leakage inductance of the transformer. V_i and v_o are the input and output voltages of a module.
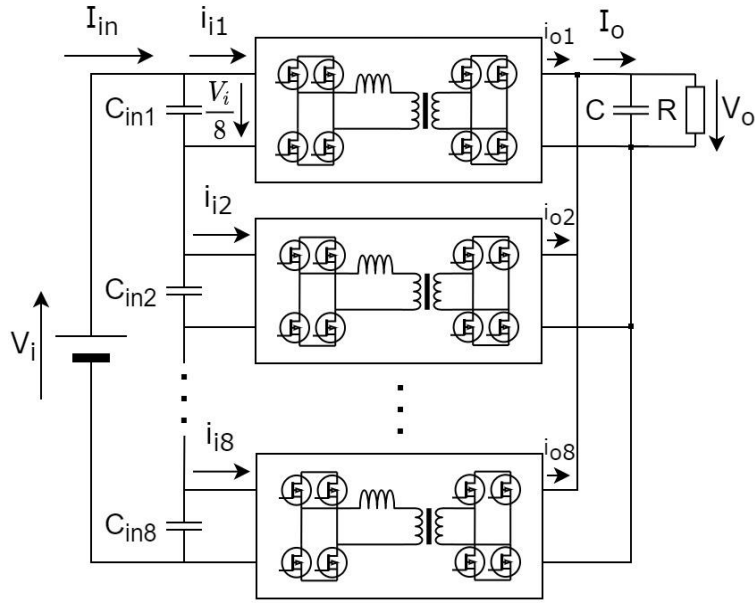
14

Fig. 10 – The eight DAB converter modules in ISOP connection.

The system's equations demonstrate that the electrical quantities of the converters and the control signals are interdependent, and that the voltage distribution is influenced by parasitic components. The suggested method is the decoupling of control variables in order to establish a distinct control loop for each module while maintaining ZVS capabilities.

Modelling the DAB converters in ISOP connection, each bridge can be considered a dependent current source:

$$
\begin{cases}
\hat{\imath}_{oj} = \left.\dfrac{\partial i_{o_{avg}}}{\partial d}\right|_0 \hat{d} + \left.\dfrac{\partial i_{o_{avg}}}{\partial v_i}\right|_0 \hat{v}_i = g_{od} \cdot \hat{d} + g_{ov_i} \cdot \hat{v}_i \\[4mm]
\hat{\imath}_{ij} = \left.\dfrac{\partial i_{i_{avg}}}{\partial d}\right|_0 \hat{d} + \left.\dfrac{\partial i_{i_{avg}}}{\partial v_o}\right|_0 \widehat{v_o} = g_{id} \cdot \hat{d} + g_{iv_o} \cdot \widehat{v_o}
\end{cases}
\tag{4}
$$

, where j is the module number and g$_{od}$, g$_{id}$, g$_{ovi}$ and g$_{ivo}$ are:

$$
g_{od} = \frac{v_i T (1 - 2d)}{n L_{lk}} = \frac{v_o (1 - 2d)}{(1 - d) d R}
$$

$$
g_{id} = \frac{v_o T (1 - 2d)}{n L_{lk}} = \frac{v_o{}^2 (1 - 2d)}{v_i (1 - d) d R} = \frac{v_o}{v_i} g_{od}
\tag{5}
$$

$$
g_{ovi} = g_{ivo} = \frac{T d (1 - d)}{n L_{lk}} = \frac{v_o}{v_i R}
$$

Assuming that all the modules have the same component values (leakage inductance, transformer turn ration, switching period and input capacitors), input voltage (V$_{in}$=v$_{in}$/8) and time-shift of bridge control signals (d). Although the perturbations are different for each $(\widehat{d_1} \neq \widehat{d_2} \neq \cdots \neq \widehat{d_8})$. In the model a resistive load is used, therefore the output voltage perturbation is obtained by multiplying the impedance of the output capacitor in parallel with the resistive load by the total output current. Considering the total input voltage constant, then the sum of input voltages will be zero, since it is equal to the total input voltage. Calculating then the output voltage, the total input current, input voltage, the converter equations can be summed up in a matrix form – (8). The detailed deduction and calculations can be found in the thesis, chapter 3.3.5. Finally, N-1 (N being the number of modules) input voltages regulated by distinct control loops and another loop for the output voltage make up the control method chosen to decouple the variables. A(s) is a variable that is defined to summarize the model equations:

$$A(s) = \frac{g_{id}}{8C_i s} = \frac{1}{8C_i s} \frac{T}{L_{lk} \cdot n} V_o (1 - 2d) \tag{6}$$

The input voltages for the modules are:

$$\begin{cases} \widehat{v_{l1}} = A(s) \cdot \left(\widehat{d_2} + \widehat{d_3} + \cdots + \widehat{d_8} - 7 \cdot \widehat{d_1} \right) \\ \widehat{v_{l2}} = A(s) \cdot \left(\widehat{d_1} + \widehat{d_3} + \cdots + \widehat{d_8} - 7 \cdot \widehat{d_2} \right) \\ \vdots \\ \widehat{v_{l7}} = A(s) \cdot \left(\widehat{d_1} + \cdots + \widehat{d_6} + \widehat{d_8} - 7 \cdot \widehat{d_7} \right) \end{cases} \tag{7}$$

Finally, using (7), the model equations are summarized in:

$$\begin{bmatrix} \widehat{v_{l_1}} \\ \vdots \\ \widehat{v_{l_7}} \\ \widehat{v_o} \end{bmatrix} = \begin{bmatrix} -7A(s) & \cdots & A(s) & A(s) \\ \vdots & \ddots & \vdots & \vdots \\ A(s) & \cdots & -7A(s) & A(s) \\ G_{vd}(s) & \cdots & G_{vd}(s) & G_{vd}(s) \end{bmatrix} \cdot \begin{bmatrix} \widehat{d_1} \\ \widehat{d_2} \\ \vdots \\ \widehat{d_8} \end{bmatrix} = H(s) \cdot \begin{bmatrix} \widehat{d_1} \\ \widehat{d_2} \\ \vdots \\ \widehat{d_8} \end{bmatrix} \tag{8}$$

In (8) all the controlled quantities are affected by the variation of the normalized phase-shifts $\widehat{d_j}$, forming a multiple input multiple output system, in which the quantities and signals are interdependent. The system must be manipulated to consider each module a single input single output system. This can be achieved by applying the aforementioned control strategy. If the H(s) matrix would be diagonal, each control signal would control a single quantity and each control quantity will depend on one signal only. Therefore, H(s) will be decomposed into a diagonal matrix D(s) and a transition matrix Y(s):

$$\begin{bmatrix} \widehat{v_{l_1}} \\ \vdots \\ \widehat{v_{l_7}} \\ \widehat{v_o} \end{bmatrix} = \begin{bmatrix} 8A(s) & 0 & \cdots & 0 \\ 0 & 8A(s) & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 8G_{vd}(s) \end{bmatrix} \cdot Y(s) \cdot \begin{bmatrix} \widehat{d_1} \\ \widehat{d_2} \\ \vdots \\ \widehat{d_8} \end{bmatrix} = \begin{bmatrix} 8A(s) & 0 & \cdots & 0 \\ 0 & 8A(s) & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 8G_{vd}(s) \end{bmatrix} \cdot \begin{bmatrix} \widehat{x_1} \\ \widehat{x_2} \\ \vdots \\ \widehat{x_8} \end{bmatrix} \tag{9}$$

It is necessary to compute Y(s) and its inverse matrix to get the control variables d as a function of the control variables x in order to observe how the new set of control variables interacts with the original ones. After doing the calculations, the normalized time shifts (d_i) as a function of the new set of variables (x_i):

$$\begin{bmatrix} \widehat{d_1} \\ \widehat{d_2} \\ \vdots \\ \widehat{d_8} \end{bmatrix} = Y(s)^{-1} \cdot \begin{bmatrix} \widehat{x_1} \\ \widehat{x_2} \\ \vdots \\ \widehat{x_8} \end{bmatrix} = \begin{bmatrix} -1 & \cdots & 0 & 1 \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \cdots & -1 & 1 \\ 1 & \cdots & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} \widehat{x_1} \\ \widehat{x_2} \\ \vdots \\ \widehat{x_8} \end{bmatrix} = \begin{bmatrix} \widehat{x_8} - \widehat{x_1} \\ \vdots \\ \widehat{x_8} - \widehat{x_7} \\ \widehat{x_1} + \widehat{x_2} + \cdots + \widehat{x_8} \end{bmatrix} \tag{10}$$

Based on this result, for the 8 modules system the decoupled control can be designed as shown in Fig. 11, where $d_1 = x_8 - x_1$, $d_2 = x_8 - x_2$, ... , $d_7 = x_8 - x_7$ and $d_8 = x_1 + x_2 + ... + x_8$:
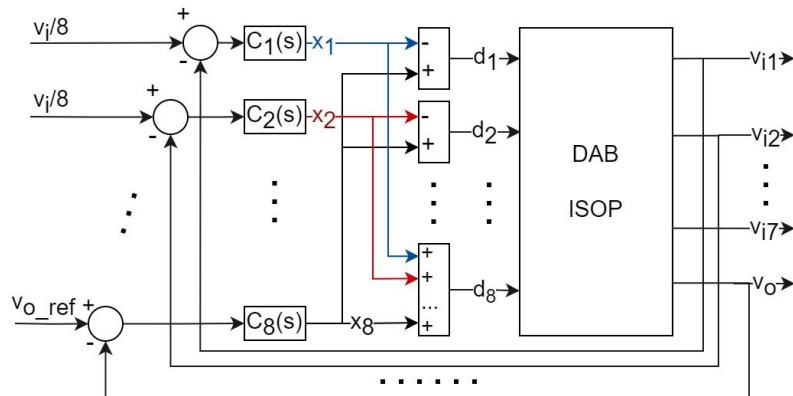

Fig. 11 – Control scheme of decoupled loops for an eight modules system.

The full-scale system with DAB modules was implemented with decoupled control as well.

Bidirectional Phase Shift Full Bridge Converter

The converter can regulate voltage over a wide range and is galvanically isolated. It has a high efficiency [22]–[24] due to the primary side's soft switching capability. The layout is asymmetric due to the employment of a filter inductor on the secondary side, however. The main issue with PSFB converters is the high voltage spike on the secondary switching components. A common solution to this issue is a diode clamp circuit [25], [26].

The BPSFB converter has the following advantages:

- It possesses ZVS characteristics on the positive power flow direction and ZCS characteristics on the negative power flow direction.
- It performs well in terms of stability and dynamic response and offers high efficiency performance regardless of the direction of power flow.
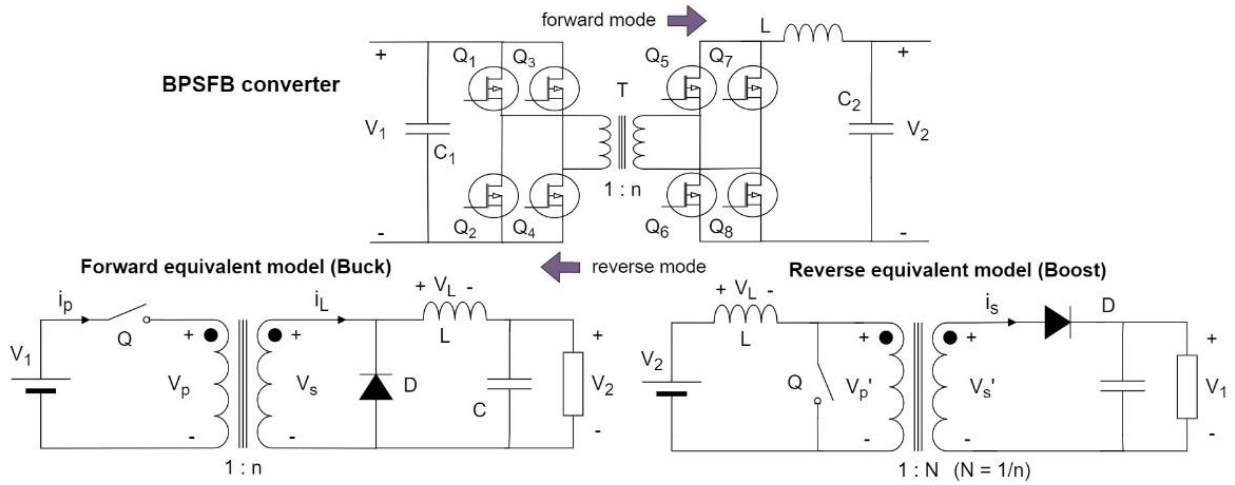
Fig. 12 – The bidirectional phase-shift full-bridge converter circuit.

Having the output inductor, this DC-DC converter topology (shown in *Fig. 12*) is asymmetric. The converter is a voltage mode full-bridge converter when the voltage is transferred from V_1 to V_2. It is a current mode full-bridge converter when the voltage is transferred from V_2 to V_1, where V_1 signifies high voltage and V_2 denotes low voltage. Containing nonlinear components such as power switches and diodes, the circuit is a nonlinear time-varying system. To obtain the converter model, it is important to simplify the complex physical model using mathematical methods. The method of small-signal analysis is suitable for linearizing nonlinear systems and deriving transfer functions. Using classical control theory, a closed-loop controller will then be developed. From an operational standpoint, this topology is fundamentally a galvanically separated buck-boost converter [27]. With the ratio of the transformer (1:n) added to the circuit, the forward mode (voltage mode) will be equivalent to a Buck converter, whereas in reverse mode (current mode) the energy transfer is identical to that of a Boost converter. Since the mathematical model of the Buck converter is well-known, it will not be deduced here. The following equation represents the open loop input-to-output transfer function for this voltage-controlled converter.

$$H_{BPSFB_{buck_o}}(s) = \frac{\widehat{v_o}}{\widehat{v_i}} = \frac{1}{1+\frac{r_L}{R}} \cdot \frac{1 + r_C C s}{\frac{s^2}{\omega_o^2} + \frac{s}{Q\omega_o} + 1} \tag{11}$$

Then, the control to output transfer function is:

$$H_{BPSFB_{buck_d}}(s) = \frac{\widehat{v_o}}{\widehat{d}} \cong H_0 \cdot \frac{1 + \frac{s}{\omega_z}}{\frac{s^2}{\omega_o^2} + \frac{s}{Q\omega_o} + 1} \tag{12}$$

$$where \quad \omega_z = \omega_{ESR} = \frac{1}{r_c C}; \quad \omega_o = \sqrt{\frac{1}{LC}\frac{1+\frac{r_L}{R}}{1+\frac{r_C}{R}}} \approx \frac{1}{\sqrt{LC}};$$

$$H_0 = \frac{nV_1}{1+\frac{r_L}{R}} \quad and \quad Q = \sqrt{\frac{LC\left(1+\frac{r_L}{R}\right)\left(1+\frac{r_C}{R}\right)}{\frac{L}{R}+C\left(r_C+r_L+\frac{r_L r_C}{R}\right)}} \approx R\sqrt{\frac{C}{L}} \tag{13}$$

In this thesis, the transfer function was manipulated into this form (with Q – damping factor), including the component parasitics.

Similarly, since the boost converter is well-known, its transfer function will not be developed in this section. See the transfer functions from input to output in the following equation, also manipulated into the damping-factor form, taking into account the parasitics.

$$H_{BPSFB_{boost_d}}(s) = \frac{\widehat{v_o}}{\widehat{d}} \cong H_0 \frac{\left(1+\frac{s}{\omega_{z_1}}\right)\left(1-\frac{s}{\omega_{z_2}}\right)}{\frac{s^2}{\omega_0{}^2}+\frac{s}{\omega_0 Q}+1} \tag{14}$$

The transfer function, (14), consists of a double-pole, right halp plane (RHP) zero and equivalent series resistance (ESR) zero. See their equation and the damping factor Q in (15).

$$\begin{cases} \omega_{z_1} = \omega_{ESR} = \frac{1}{r_c C} \quad and \quad \omega_{z_2} = \omega_{RHP} = \frac{(1-D)^2(R-r_L)}{LN^2} \approx \frac{R}{LN^2}\left(\frac{V_2}{V_1}\right)^2 \\[4mm] \omega_0 = \frac{1}{\sqrt{LC}}\sqrt{\frac{r_L+(1-D)^2 R}{R}} \approx \frac{1-D}{\sqrt{LC}} \quad or \quad \frac{1}{\sqrt{LC}}\frac{V_2}{V_1} \\[4mm] Q = \frac{\omega_0}{\frac{r_L}{L}+\frac{1}{C(R+r_C)}} \approx (1-D)R\sqrt{\frac{C}{L}} \\[4mm] H_0 = \frac{V_2 N}{(1-D)^2} = \frac{NV_1{}^2}{V_2} \end{cases} \tag{15}$$

PID Compensator Design

Before building the control loop, the frequency-domain method [28] was be used to determine the proportional-integral-derivative (PID) parameters and to implement a Mathcad design sheet (*Fig. 13*. For that, the following input conditions were defined and met:

1. The phase margin should be greater than 45°. Let $\varphi_m = 70°$.
2. At cut-off frequency $\omega_c = \omega_{sw}/10$, the gain of the open loop transfer function should be unitary: $|T(j\omega_c) = 1|$.
3. The zero's frequency introduced by the integrative component must be sufficiently low so as not to impact the phase (arg(T(jωc)) of the open loop transfer function at the cut-off frequency fc. It is advised to set: $\omega_{Z_{PI}} = \omega_c/10$.
4. The frequency of the pole introduced by the derivative part is recommended to be $\omega_{P_{PD}} = \omega_{sw}/2$. This however, can be changed as necessary.

An equivalent analog PID controller was also designed. In simulation both digital and analog control was tested for both the selected converter topologies. Finally digital control was chosen and the equivalent difital filtered PID parameters were deduced, applying Tustin discretization.

$$f_c := \frac{f_{sw}}{10} = 1 \times 10^4 \frac{1}{s} \qquad \varphi_m := 70 \cdot \frac{\pi}{180} = 1.222$$

input parameters

resulting PID parameters

$$\omega_c := 2\pi f_c = 6.283 \times 10^4 \frac{1}{s}$$

$$\omega_{Z\_PI} := \frac{\omega_c}{\tan\left(\varphi_m - \pi - \arg\left(H_{PSFB\_d}(j \cdot \omega_c)\right) + \operatorname{atan}\left(\frac{\omega_c}{\omega_{P\_PD}}\right)\right)}$$

$$\omega_{Z\_PD} := \frac{\omega_c}{10}$$

$$\omega_{P\_PD} := \pi f_{sw}$$

$$T_f := \frac{1}{\omega_{P\_PD}} \qquad T_f = 3.183 \times 10^{-6} s$$

$$k_P := k_I \frac{\omega_{Z\_PI} + \omega_{Z\_PD}}{\omega_{Z\_PI} \cdot \omega_{Z\_PD}} - k_I \cdot T_f$$

$$k_I := \frac{\omega_{Z\_PD}}{\left|H_{PSFB\_d}(j \cdot \omega_c)\right|} \cdot \frac{\sqrt{1 + \left(\frac{\omega_c}{\omega_{P\_PD}}\right)^2}}{\sqrt{1 + \left(\frac{\omega_c}{\omega_{Z\_PI}}\right)^2}}$$

$$k_D := \frac{k_I}{\omega_{Z\_PI} \cdot \omega_{Z\_PD}} - k_P \cdot T_f$$

$$P := k_P = 0.047$$

$$H_{PID}(s) := k_P + \frac{k_I}{s} + \frac{k_D \cdot s}{T_f \cdot s + 1}$$

$$I := k_I = 290.623 \frac{1}{s} \qquad k_D = 4.349 \times 10^{-8} s$$

$$H_{comp}(s) := H_{PID}(s) \cdot H_{PSFB\_d}(j \cdot \omega_c)$$

$$N_{PID} := \frac{1}{T_f} = 3.142 \times 10^5 \frac{1}{s}$$

Fig. 13 – Design equations resulting the tuning parameters.

A Novel Regenerative Active Clamping Snubber
– comparison with two other classic snubbers –

For a high-power converter to be efficient, switching losses must be minimized. By exploiting parasitic capacitance and leakage inductance, Zero-Voltage-Switching (also known as soft switching) can be obtained, hence reducing switching losses. The problem with these converters with high output voltage is secondary side parasitic ringing. These occur-rences generate significant stress on the diodes, necessitating a snubber clamping circuit to mitigate this problem. In high-power and high-frequency applications, traditional RC snubbers return energy to the output with major losses. RDC clamped snubbers present acceptable losses, utilizing a capacitor as a constant voltage tank (if the average current through the clamping capacitor is zero at steady state) to obtain an additional discharge path and recover a portion of the snubber loss at the output. Such a snubber circuit cannot be designed without compromise, as the energy dissipated through the resistor remains high at greater output power levels, causing the circuit's efficiency to decrease [29]–[33].

Regenerative active clamping (RAC) snubbers with additional active and passive components, however, are a good alternative. It includes an additional current path that allows the clamping capacitor to charge the output capacitor. Using a buck converter, the proposed technique transfers the energy losses to the output. The MOS transistor Q_s, diode D_s, capacitor C_s, and inductor L_s that make up its structure are highlighted in a red frame in *Fig. 14*.

This snubber circuit, along with two other traditional snubbers, is connected to a full-bridge phase-shift converter with a diode rectifier on the secondary side for the purpose of comparison. The leakage inductance of the transformer and the parasitic capacitances of the primary transistors are used to obtain zero voltage transition. *Fig. 15* shows the equivalent model of the PSFB converter, where V_d and L_s represent the input voltage and the equivalent of the leakage inductances as seen from the secondary side, V_s is the output of the diode rectifier, and C is the sum of the parasitic capacitances.
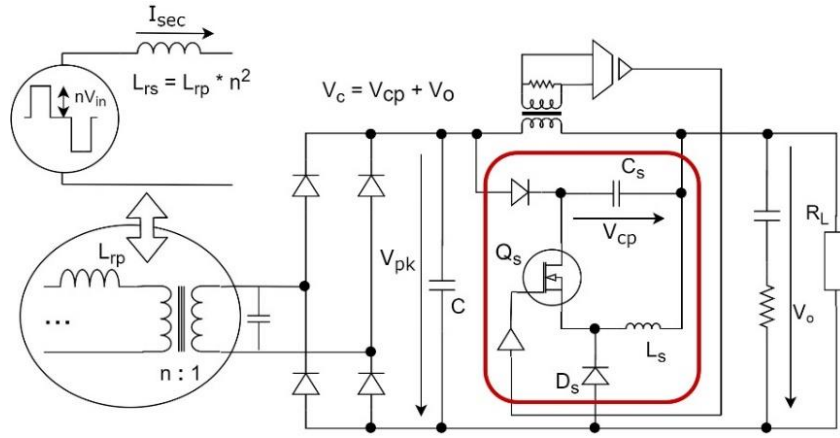
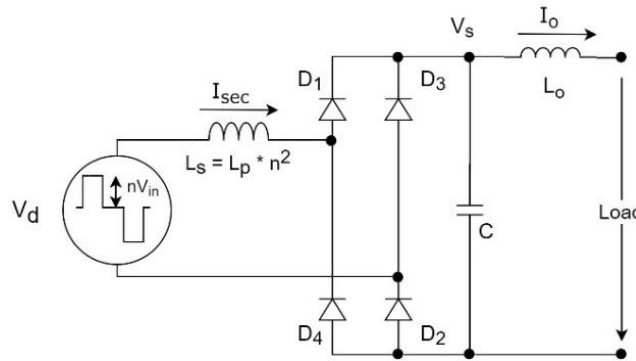Fig. 14 – *Scheme of the Regenerative Active Clamping (RAC) Snubber.*

Fig. 15 – *Phase-Shift Converter equivalent model*

When the diodes D_3-D_4 begin to conduct, I_{sec} will increase until it reaches I_o, at which point the excess current will flow into the parasitic capacitance C according to the equation $I_C = I_{sec} - I_o$. This will trigger the resonance between C and L_s, whose resonant frequency f_{ring} is:

$$f_{ring} = \frac{1}{2\pi\sqrt{L_s C}} \tag{16}$$

The output voltage and output current of the rectifier are given in (17). V_s can reach a maximum value of $2V_d$, as can be observed. This is the primary reason why snubbers are required, allowing for the use of lower voltage and less expensive rectifier diodes or transistors.

$$\begin{cases} V_s = V_d - V_d \cdot cos\dfrac{t}{\sqrt{L_s C}} \\ I_{sec} = I_o + \dfrac{V_d}{\sqrt{\dfrac{L_s}{C}}} \cdot sin\dfrac{t}{\sqrt{L_s C}} \end{cases} \tag{17}$$

Fig. *16* shows the high-amplitude voltage oscillation caused by the resonance reaching as high as $2 \cdot V_d$. On the prototype converter, this waveform was measured with no snubber circuit connected.
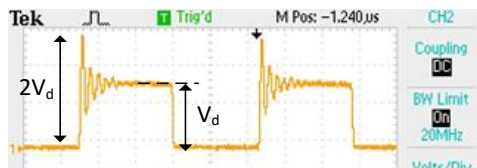
Fig. 16 – *Ringing caused oscillation in the secondary.*

The second snubber employed and analyzed to address the aforementioned issues resulting from the previously described ringing effect is the classical RDC snubber as on *Fig. 17*.
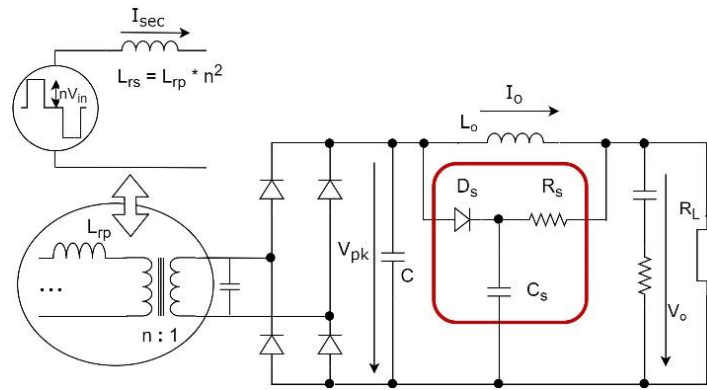
Fig. 17 – *Phase-Shift converter with RDC snubber.*

Passive RDC snubbers, are a simple, inexpensive and robust solution that can be used in a variety of applications. However, when the output power increases, R_s can dissipate a substantial amount of energy, hence decreasing the system's efficiency.

The second snubber to be discussed is one with clamping diodes (CD) on the primary side, as presented in *Fig. 18* below:
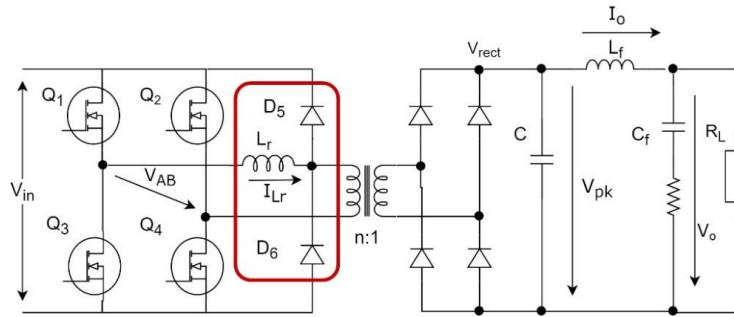
Fig. 18 – *Phase-Shift converter with clamping diodes.*

This arrangement is based on the creation of a commutating aid circuit consisting of two diodes and a small inductor to reduce the effect of ringing and high amplitude voltage without introducing additional power device control system and losses.

Regenerative Active Clamping Snubber

The fact that the control signals for the snubber transistor are obtained from the primary side MOFET driving signals is one of the challenges posed by this sort of snubber. This signal must be utilized on the secondary side, which necessitates additional control logic and galvanic separation. Furthermore, an expensive high-voltage film capacitor is required. However, the snubber described in this study, modified from [34] as shown in *Fig. 14*, uses a simple secondary winding on the output inductor to create a novel MOSFET transistor drive technique. In addition, a novel step-by-step design approach (including a complete mathematical model) and a PSIM simulation model are proposed in this chapter. Using the primary leakage inductance reflected in the secondary – L_r, and the total secondary parasitic capacitance (of the transformer and rectifier bridge) – C, resonance is achieved. The thesis includes the detailed mathematical model with all equation deductions for both discontinuous and continuous buck operation modes also offering a well-defined design procedure, including a design example. Depending on the input voltage range, the duty cycle will vary. With the minimum duty cycle value, the snubber inductor can be determined – (18) – for the case of limit of conduction for a certain V_{cp}. V_{cp} can be determined for discontinuous mode by tracing L_s in this operating mode – (19) as a function of v_{cp} and using the previously defined inductor value, as Fig. *19* illustrates. Table 4 – RAC snubber summary. presents a short summary of this snubber circuit and its advantages and disadvantages.

$$L_{S_{discontinuous}} = \frac{(V_{cp} + V_o - V_{in})V_{cp}(1-D)^2 T^2}{(V_{cp} + V_o)(2V_{in} - V_{cp} - V_o)C} \tag{18}$$

$$L_{S_{continuous}} = \frac{(V_{cp} + V_o - V_{in})V_o{}^2 D T^2}{(V_{cp} + V_o)^2 (2V_{in} - V_{cp} - V_o)C} \tag{19}$$
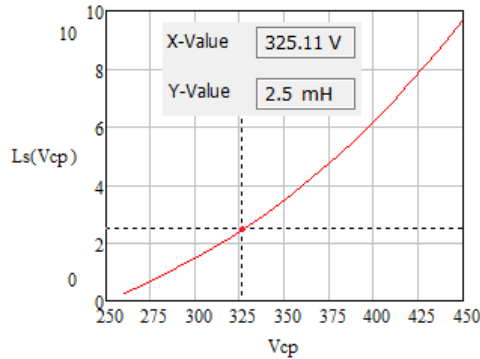

Fig. 19 – *Snubber inductor as a function of snubber capacitor voltage.*

Table 4 –RAC snubber summary.

advantages	disadvantages
• The control mechanism uses a secondary winding on the output inductor to generate the signal necessary to drive the snubber transistor; • Well-defined design process; • Transfers the energy losses to the output and low power loss.	• High values for the snubber inductor (in the mH range); • High saturation current for this inductor (usually higher than 1A); • Higher circuit complexity and higher costs.
It is a good solution for high-power converters with high output voltage.	

RDC Snubbers

RDC snubbers are generally preferred to conventional RC snubbers due to their acceptable losses. On Fig. *17* C_S is regarded as a constant voltage source with amplitude Vcs that absorbs the energy of stray inductances during the switch-off time. When the rectifier output voltage V_S reaches Vcs, the snubber diode D_S will open and conduct to provide a path for the surplus current I_{sec} - I_o. The resistor is required to provide a discharge path to the snubber capacitor C_S in order to maintain charge balance and also to recover loss to the output. In the thesis the mathematical model and design equations are deduced for this snubber as well.

It is evident that this setup involves a trade-off between power loss and the level of clamping, hence it is only practical up to moderate power levels. In addition, a high voltage capacitor and diode are required. The most significant of its advantages are its robustness, simplicity, and cost-effectiveness.

Table 5 –RDC snubber summary.

advantages	disadvantages
• Simplicity, robustness and low cost.	• Compromise between loss and the amount of clamping. • High voltage capacitor and diode are needed.
It is useful only up to medium power levels	

Clamping Diode Snubbers

This snubber concept is basically a commutating aid circuit consisting of the two diodes and a small inductor to reduce the ringing and high amplitude voltage, without introducing additional control of power devices and losses, as seen on Fig. *18*. It also extends the soft switching interval at light loads. D_5 and D_6 clamps the rectifier output voltage at its reflected input voltage to eliminate the high-amplitude voltage oscillation, without introducing losses. By connecting the resonant inductor to the lagging leg of switching transistors instead of the leading leg, the clamping diodes will conduct only once instead of twice, in a switching period, therefore the resonant current is decreasing being equal with the primary, reducing the conduction loss in primary side. The current rating of the clamping diodes can also be lowered. Table 6 is a short summary about this snubber.

Table 6 –RAC snubber summary.

advantages	disadvantages
• Reduces the resonant inductor current, improving efficiency; • Lower voltage diodes can be used for clamping; • Extends the soft switching range toward light-load scenarios; • Having a separate resonance inductor, there is no need to carefully design a large leakage inductance inside the transformer.	Even so, this inductance together with the parasitic capacitances of the rectifier diodes can cause ringing that must be addressed.
Suited for converters where the resonant inductor is not embedded in the power transformer.	

Snubbers Comparison – simulation and experimental results

PSIM was used to create a simulation model to compare the three snubber circuits. The model includes both the power stage and control loop. The converter is a battery charger capable of exceeding 3000 W, shown on *Fig. 20*. The shaded areas represents the snubber circuits, which are tested individually, and the results are compared. The snubber transistor's method of control is an original concept. Novelty resides in the employment of a secondary winding on the output inductor to provide the signal needed to command the MOSFET transistor.
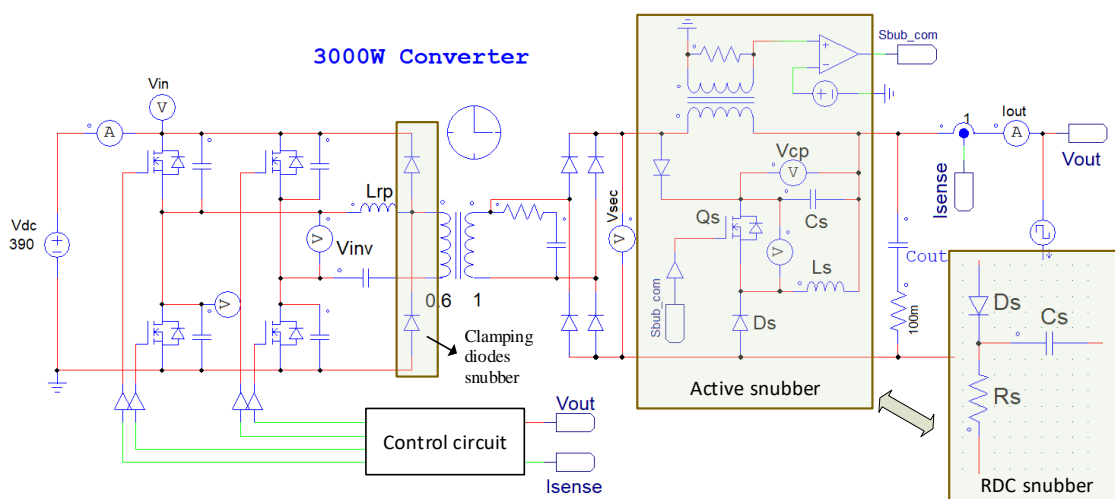
Fig. 20 – The schematic of the phase-shift converter with the three different snubber circuits.

Following the design procedure presented in the thesis, the following component values resulted for the RDC snubber: R_s = 39kΩ, C_S = 33nF/1000V and a SiC diode with V_{br} =1200V. The clamping voltage V_{cs} was 750V and the power dissipated by the snubber resistor was 14W.
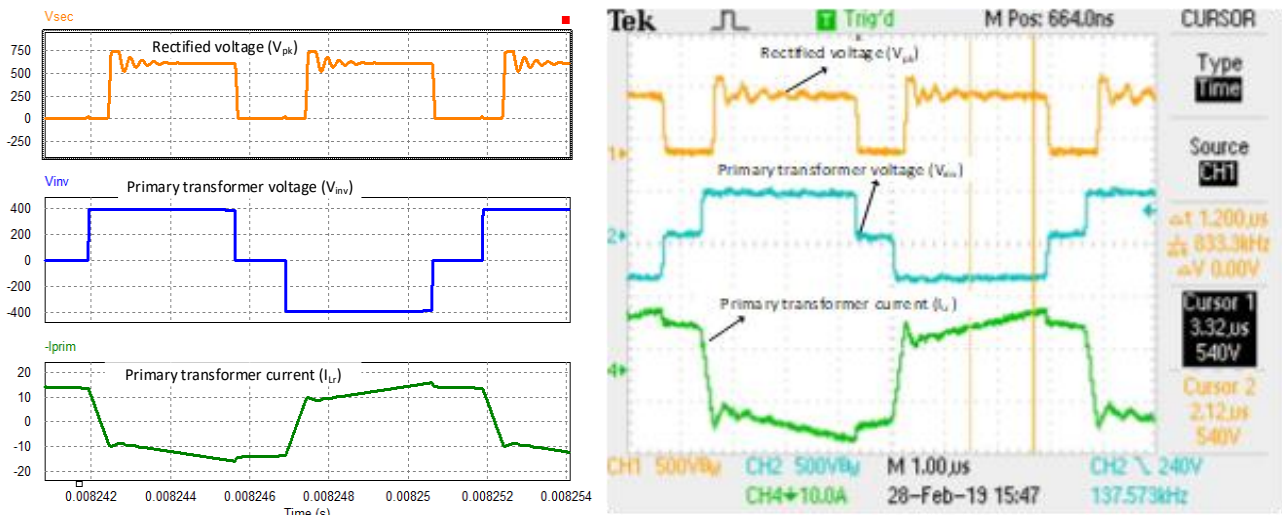
Fig. 21 – RDC snubber simulation (on the left) and experimental (on the right) results.

Regarding the Clamping Diodes snubber, on Fig. 22 it can be observed, as mentioned earlier, that the transformer lag configuration is more advantageous because the diodes conduct only once in a switching cycle reducing power dissipation of this diodes.
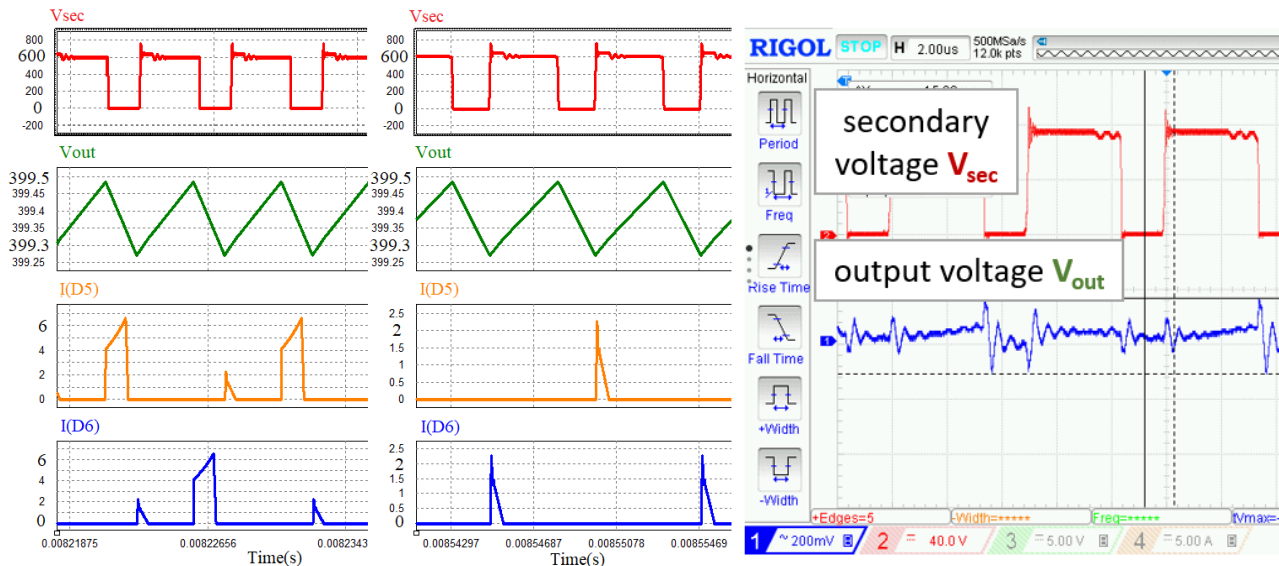

Fig. 22 – CD snubber simulation and experimental results. For the simulation results, on the left is the transformer lead configuration and on the rigth the transformer lag configuration.

Finally, the buck-converter from the RAC snubber is controlled by a duty cycle that is anti-phase to the duty cycle of the phase-shift converter, with $D_{snubber} = 1 - D_{phase-shift}$. Fig. *23* depicts the secondary voltage (up), the current through the snubber inductor (center), and the current through the snubber capacitor and transistor (bottom). As predicted by the mathematical model, the mean values of I_{Cs} and I_{Qs} are identical (the two shaded regions). The values resulted from the design procedure are: L_s=1mH/1A saturation current, C_s=33nF/1000V, the diodes are SiC diodes with V_{br} =1200V and the transistor is a MOSFET transistor with V_{ds} = 950V, and I_D =3A. The simulation data are shown in Fig. *24*a. In this scenario, the rectified voltage was limited to 600V and active snubber losses are minimal. The experimental findings are shown in Fig. *24*b. They correspond closely to the simulation results and validate the design method. The C_s voltage is observed to be less than 1000V, and the inductor current is less than the snubber inductor's saturation current (1A). V_{ds} is also smaller than the transistor's breakdown voltage. The results demonstrate the correct operation of the snubber circuit and validate the newly developed control approach.
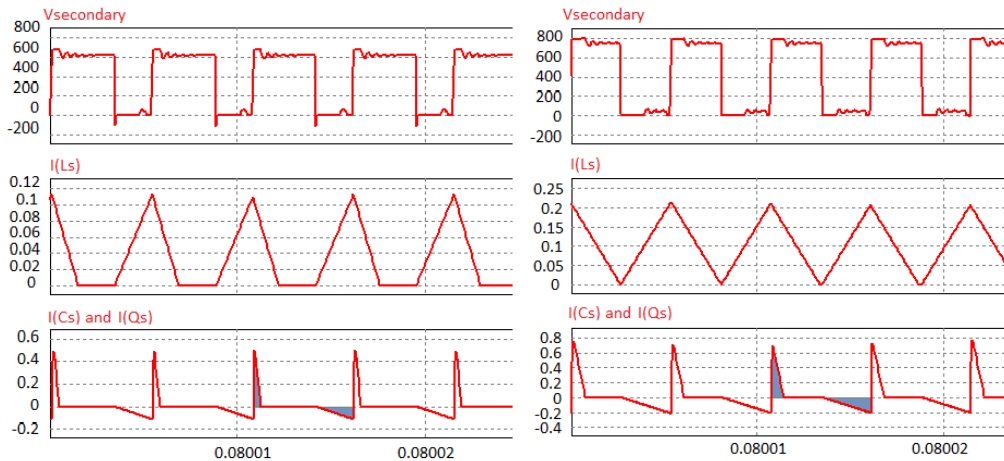
Fig. 23 – *Operation in discontinuous conduction mode (left).*
Operation at the limit of continuous conduction mode (right).

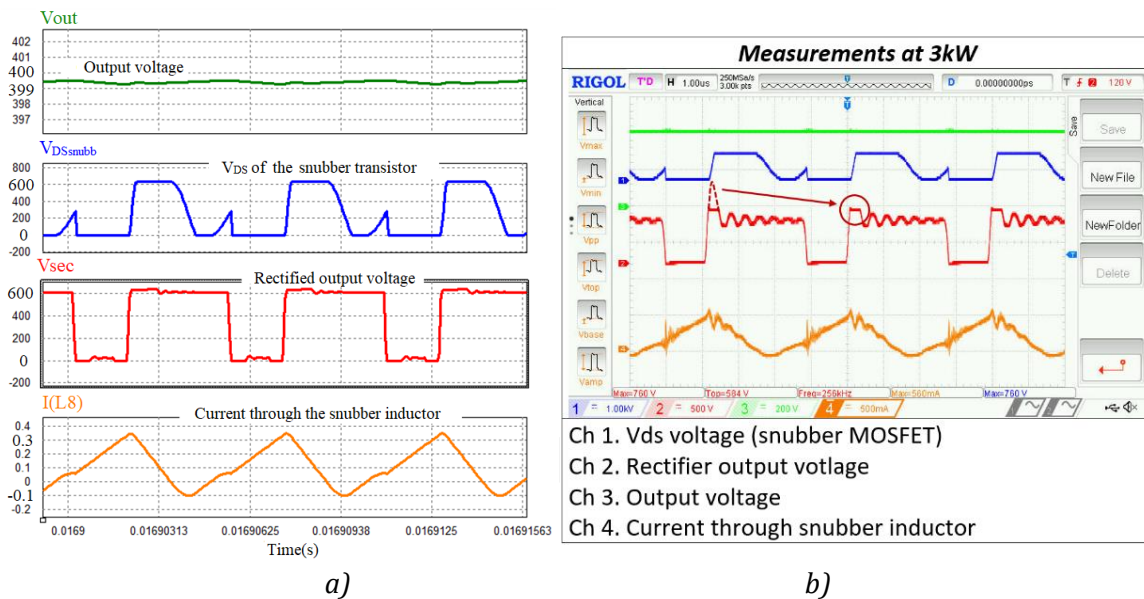*a)*   *b)*

Fig. 24 – *a) Simulation results for the regenerative active snubber. b) Experimental waveforms.*

This chapter demonstrates that all three snubber topologies are compatible with the PSFB converter. For the reported RCD and RAC snubbers, the amplitude of parasitic oscillations was lowered to less than V_{cs}, potentially decreasing EMC issues. Due to the leakage inductance of the transformer and the equivalent parasitic capacitances, the CD snubber may still exhibit parasitic oscillations, which must be mitigated. Table 7 below displays the simulated power dissipation for the three 3000 W output snubbers. In addition to its substantial power loss, the RCD snubber reduces the efficiency of the power converter. Additionally, a high-power resistor must be installed on the heatsink.

Table 7 – Comparison of losses on the three different snubbers.

RCD snubber	CD Snubber	RAC Snubber
14 W	120 mW	230 mW

The RAC snubber offers a minimal power loss and can be used with an L_r integrated in the power transformer. The suggested protection circuit provides an effective solution for high voltage spikes and energy losses, with the added benefit of moving energy loss to the output. Additionally, this concept is compatible with different high-power topologies.

Experimental and Simulation Results – comparison

This last study covers the third major stage of the project and it will present the developed software model and experimental prototype of the medium voltage DC transformers. This chapter focuses on results of the full-scale software model of the two traction systems and on the experimental module prototype of the two converters. For the sake of comparison, the exact software model of the experimental boards (small-scale) are also implemented to analyze the differences between the results obtained in the experiment and in simulation. In the thesis, this study extends the literature research about the impact of WBG semiconductors on traction systems from the first chapter with insights and results from the literature on power density and efficiency. In this way a full-scale system's efficiency and power density are estimated. Furthermore, losses evaluation method is presented for both converter topologies. A prototype of DC transformer for railway traction is implemented in this chapter. The experimental tests are focused on the verification of the operation of the system and on the control strategies developed in the previous chapter.

DAB Based PETT System

The DAB module is depicted in Fig. *25*, with the converter module's schematic on the left and its Matlab/Simulink model (with identical parameters) on the right. The converter was evaluated with an input voltage between 130-350 V and an output power on the range of 0-1000 W. The experimental setup for the results provided here is depicted in Fig. *26*. The converter was digitally controlled by a Texas Instruments control board, and a Chroma electronic load was connected to the system as the load. Experiment versus simulation will present the waveforms for two distinct loads and the response to load step changes.
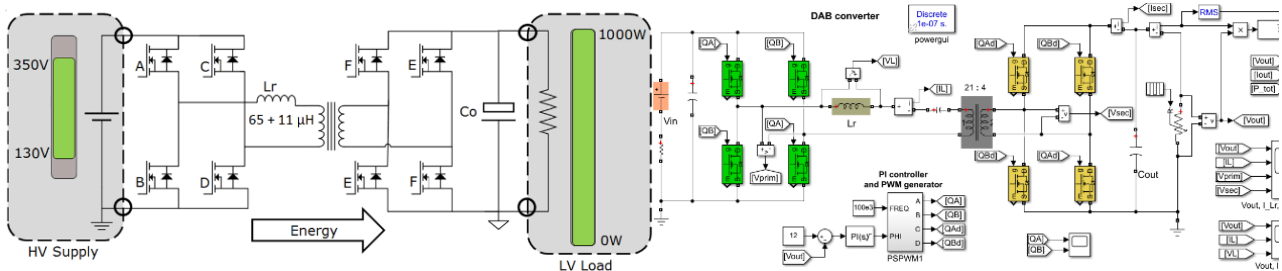
Fig. 25 – *Experimental small-scale DAB converter module (on the left) and its simulation model (right).*
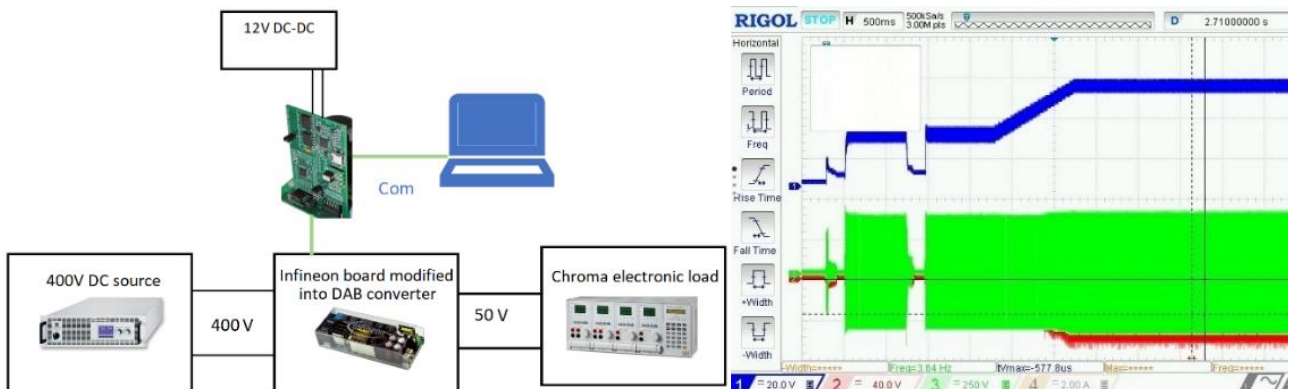
Fig. 26 – *Experimental setup of the DAB PETT module (on the left). Soft start of the converter with 300 ns dead time: channel 1 – V_o (output voltage), ch. 2 – $V_{secondary}$ (secondary voltage) and on ch. 3 – $V_{primary}$.*

Fig. *27* illustrates some significant waveforms for a 6A load current, including the output voltage variation, inductor current, and primary and secondary voltages for 300 W output power. To deliver power at varying rates, the phase-shift between the two bridges is changed,

hence altering the current and voltage waveforms of the resonant inductor. Fig. *28* depicts the current and voltage of the inductor, as well as the output voltage, for the 6A load.
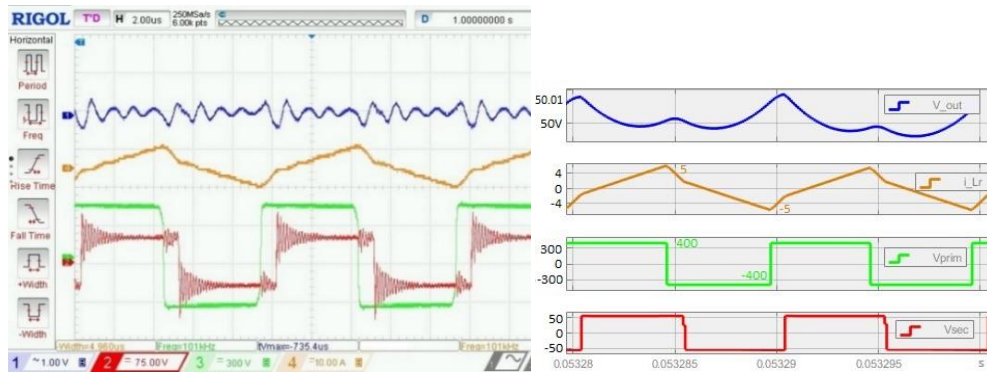

Fig. 27 – *Waveforms at 6A load current. Left side: on the oscilloscope: channel 1 – ΔV_0 (output voltage ripple), ch.2 – V_Sec, ch.3 – V_Prim, ch.4. – resonant inductor current I_Lr; Right: the same in the simulation model.*
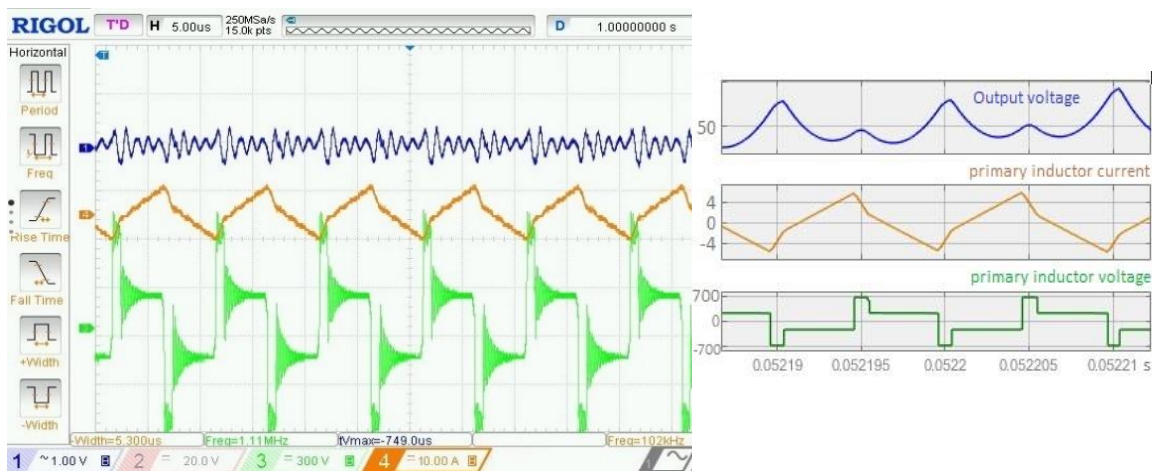

Fig. 28 – *Waveforms at 6A load current. On the left: on the oscilloscope: ch.1 – ΔV_0, ch.3 – primary inductor voltage V_Lp, ch.4. – resonant inductor current I_Lr; On the right: same waveforms in the simulation model.*
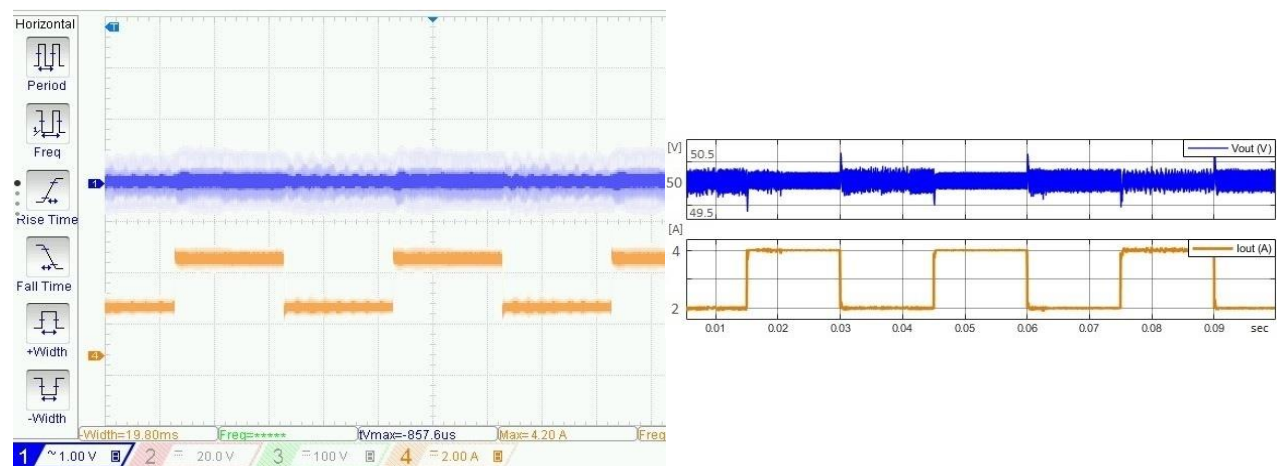
Fig. 29 – *Response to load steps: left: ch.1 – ΔV_0, ch.4 – I_0 (2A/division); right: simulation waveforms.*

Finally, the response of the system to load changes (2A steps = 100 W) was evaluated. *Fig. 29* shows a screenshot of the oscilloscope, and the simulation result. The converter is robust and has quick response. The DAB is a simple, yet powerful converter; it demonstrated steady functioning in a variety of scenarios; and it would be suited for a modular PETT system. In the conclusion section, additional conclusions will be taken.

BPSFB Based PETT System

For the BPSFB module, the same strategy was followed as for the DAB; *Fig. 30* depicts the converter scheme, and its simulation model with the identical parameters. This converter is a second-order system and is operated differently than the DAB due to the output inductor. It is digitally controlled by an Infineon board using a computer program to configure the PID parameters. *Fig. 31* depicts the arrangement of the test bench for measurements up to 1kW, and demonstrates the soft start of the module. In the thesis more measurements and figures are included, such as dead time, rising time, different load current and reverse mode operation.
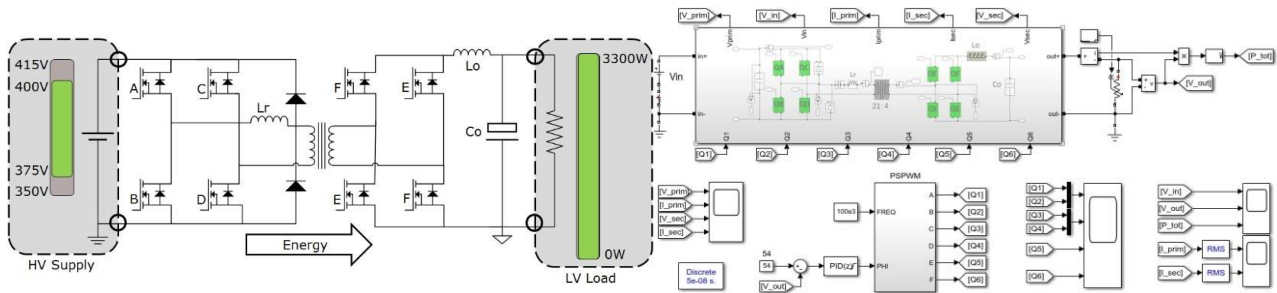
Fig. 30 – *Small-scale BPSFB module (on the left) and its Matlab/Simulink model (on the right).*
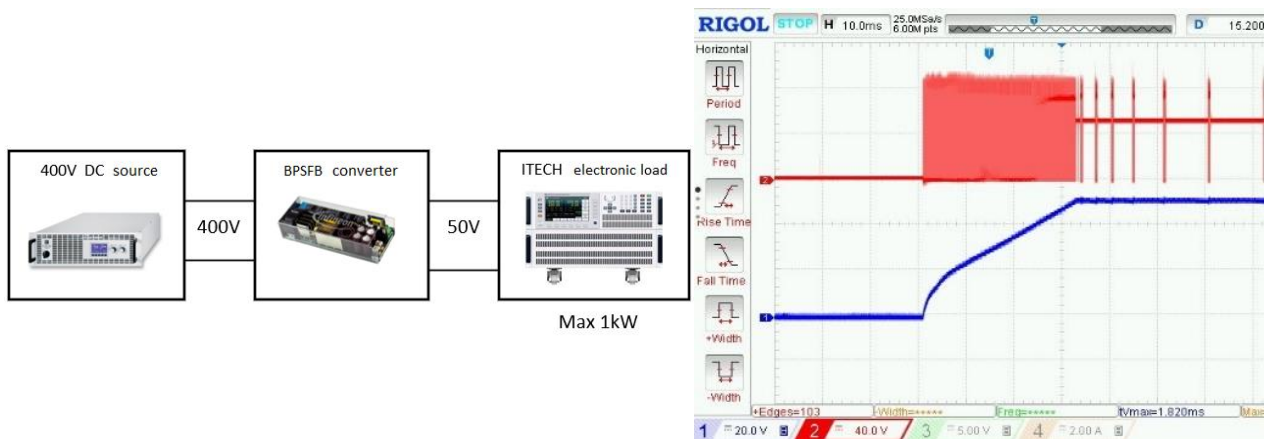
Fig. 31 – Experimental setup of the BPSFB PETT module (on the left). Soft start of the converter: channel 1 – V₀ (output voltage), ch. 2 – V_sec (secondary voltage) (on the right).

On the following figure, two load scenarios are shown. *Fig. 32* depicts the output parameters for (a) 10A load current and 500W output power, (b) the waveforms on the oscilloscope – output and secondary voltage, and inductor current; and (c) the same in the simulation model. The right column is the same, but for a 20A load current and 1kW output power. *Fig. 33* depict the output voltage and its ripple at 1 kW, as well as the rectified secondary voltage.

(a)

(b)

(c)
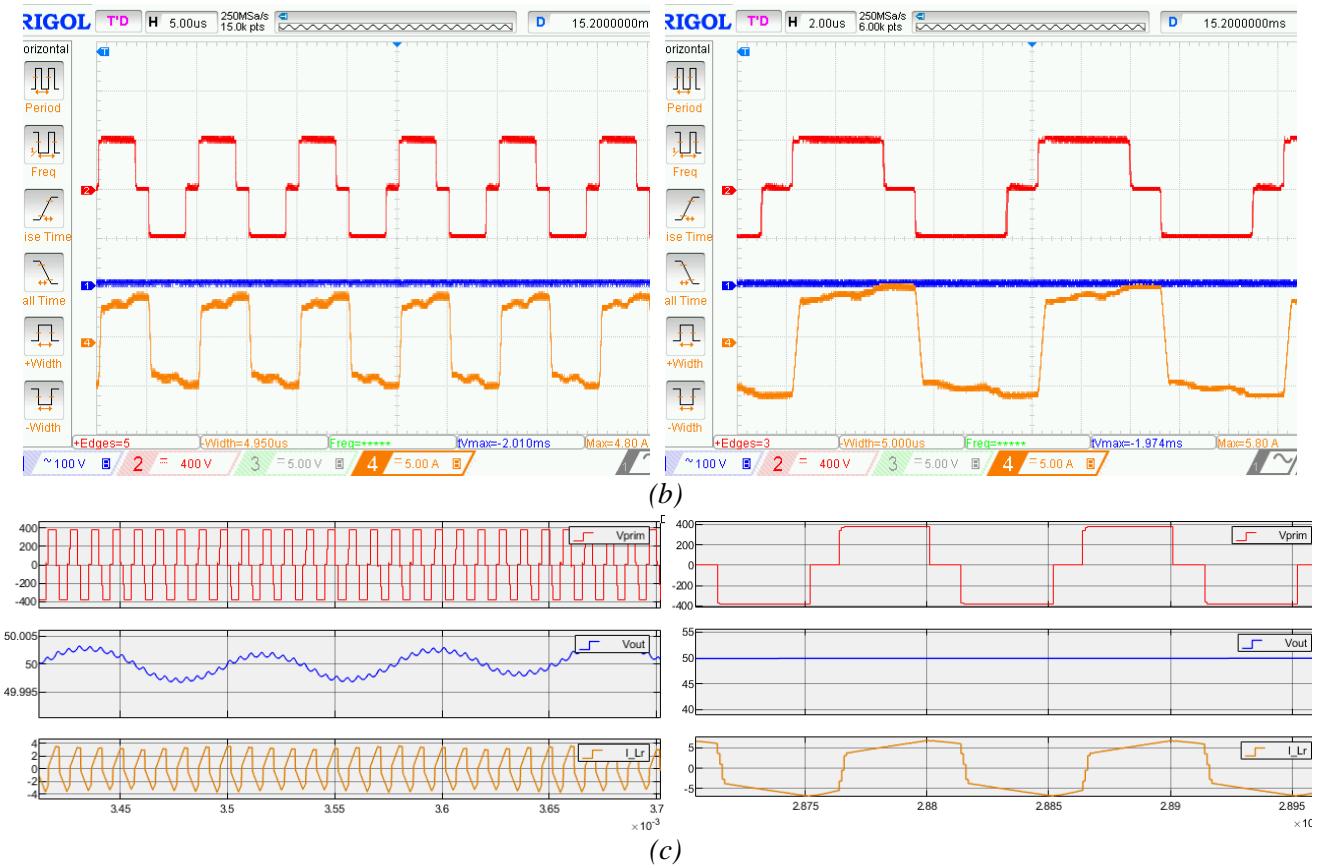
Fig. 32 – *Waveforms at (a) 5A load current and 20A respectively: (b) on oscilloscope: ch.1 – ΔVO, ch.2 –
Vprim, ch.4. – resonant inductor current I_{Lr}; (c) same waveforms in the simulation model.*
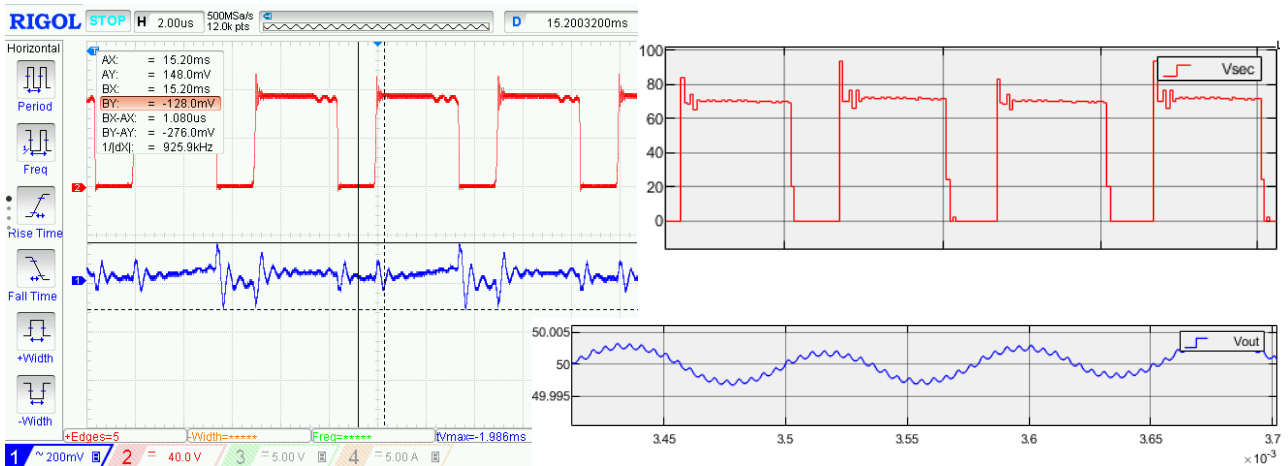

Fig. 33 – On the left: output voltage and its ripple at 1 kW: CH_1 – output voltage (300 mV peak to peak
ripple); CH_2 – secondary rectified voltage; on the right: same waveforms in the Matlab/Simulink model.

Two electronic loads were attached to the converter in order to test the system above
1000W and generate 500 W load steps. As shown in Fig. *34*, the responsiveness to load changes
was tested using 100 ms and 10 A (500 W) steps.

In similar way as presented here, in the thesis the experimental setup, simulation and
oscilloscope results are also shown for the reverse (boost) mode of the BPSFB converter. The bi-
directional PSFB converter board has been modified into a DAB converter, thus obtaining
two small-scale prototypes, as presented here. Both topologies were evaluated, and measure-
ments were compared with the Matlab/Simulink simulation model of both converters. Addi-
tionally, a synchronous electric motor was connected to the module and successfully operated
under various speed and torque settings, shown on Fig. 35 and Fig. 36.
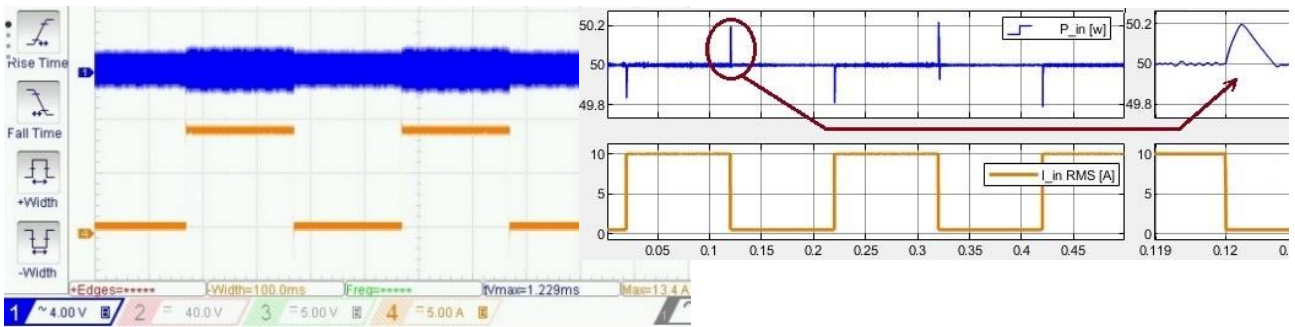
Fig. 34 – *Response to 100ms load steps: ch.1 – ΔV_0, ch.4 – I_0 steps, compared with the simulation waveforms.*
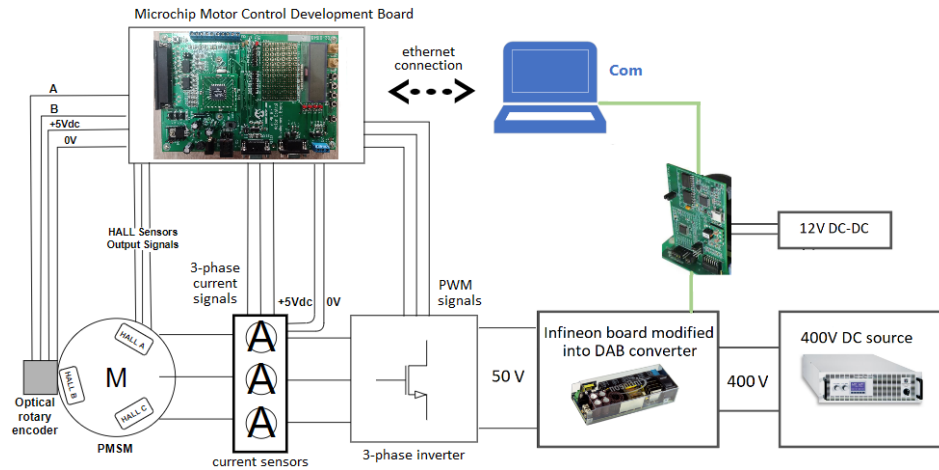

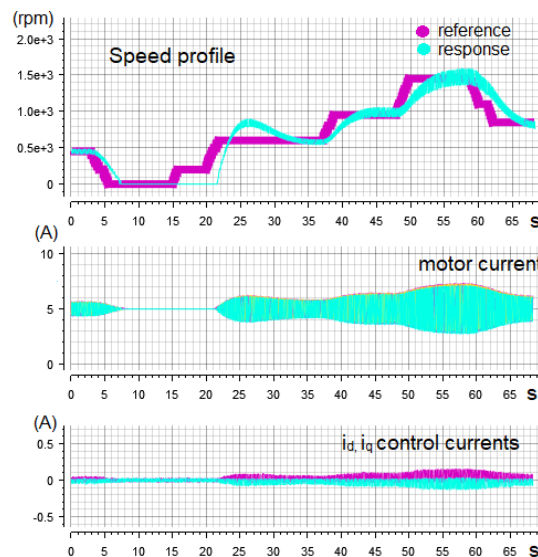Fig. 35 – *Laboratory experiment – Motor drive setup block diagram.*

Fig. 36 – *Laboratory experiment measurements – Motor drive speed profile and current waveforms.*

Monitoring was performed on the following PETT system parameters: output ripple voltage, output current and resonant inductor current. For the DAB configuration, the simulation model of the experiment prototype yielded a ripple in the output voltage between 2.5% and 3.3%, while the actual experiment yielded a ripple of 5%. 5 to 10 percent was the highest difference between the currents obtained in simulations and those measured in experimental tests for various load conditions. The highest difference between currents for the BPSFB converter was approximately 10 percent at maximum load and up to 5 percent for light loads. The ripple on the output voltage for constant power is only 300 mV of 50 V (0.6 percent). The ripple reaches a maximum of 10 percent (5 V peak to peak) in varied load scenarios with varying power. In the simulation, the ripple in the output voltage was insignificant.

Full Scale Simulation Models

On the basis of the mathematical model of the converters and using the Mathcad automated design sheets, PSIM and Matlab/Simulink were used to construct a single module of both converter sub-topologies. Following the successful simulation of the converter modules, a full-scale, eight-module version of the traction transformer was implemented in the second phase of the software model development. Table 8 displays the MVDC railway line specifications provided by University of Birmingham as partner in the project [14], [35], [36]. The full-scale PETTs based on BPSFB and DAB converter modules shown in Fig. 37 were tested on the entire voltage range of the catenary line.

Table 8 – Input voltage specifications for PETT (catenary line voltages).

Parameter	Symbol	Value (kV)
Lowest non-permanent voltage	U_{min2}	17.5
Lowest permanent voltage	U_{min1}	19
Nominal voltage	$V_{DC,nom}$	25
Highest permanent voltage	U_{max1}	27.5
Highest non-permanent voltage	U_{max2}	29
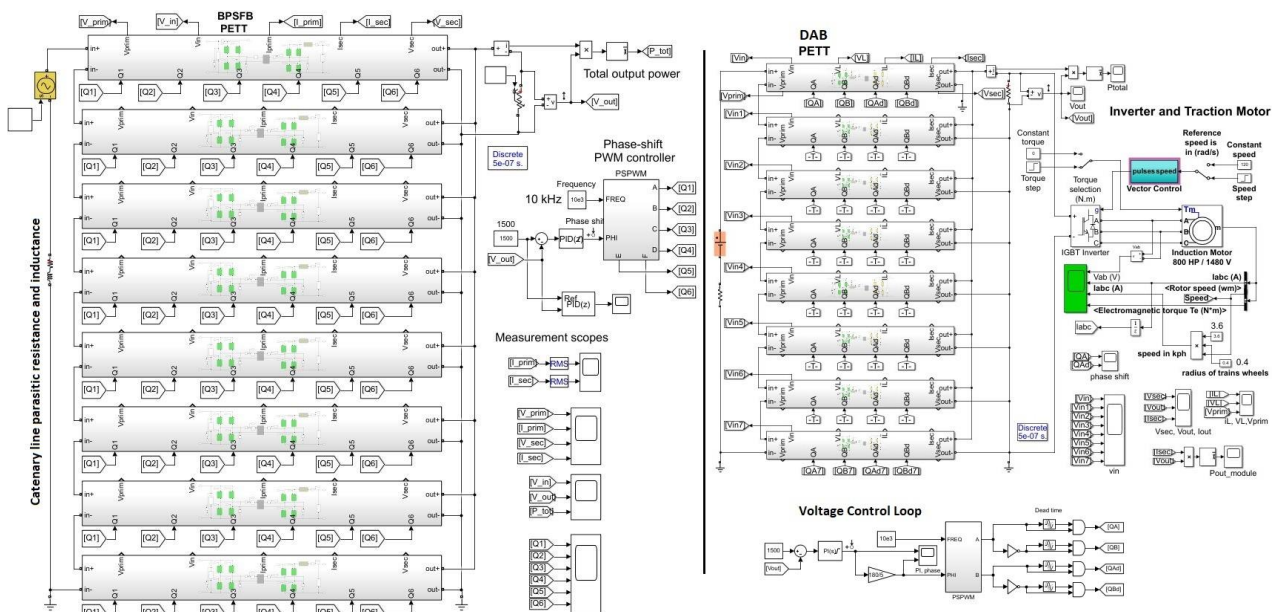
Fig. 37 –The full-scale simulation model of both DAB and BPSFB based PETT systems.

Input voltage variations from 17.5 kV to 29 kV were simulated with varying step sizes based on Table 8's MVDC catenary line parameters. On the input side, the railway line and catenary parameters were also considered: R_r – the running rails resistance, R_{cat} – catenary resistance and L_{cat} – parasitic inductance of the catenary. Running rails are connected to the negative terminal of the MMC of a subtation and provide return path for the current. Therefore the DC PETT will see ($R_{cat} + R_r$) and L_{cat}. From Table 1 of the paper [37], the parameter values are: R_{cat} = 0.5 × 0.16 Ω/km; L_{cat} = 1.55 mH/km and R_r = 15 mΩ/km. Since the nominal current for the MVDC line is 800 A, two parallel 150 mm² conductor is considered. Therefore the coefficient of 0.5 is present in R_{cat}. In this simulation 50 km distance between substations was chosen, thus a train's maximum dis-tance from a substation would be 25 km – halfway between two feeding stations. As shown in Fig. *38*, the developed voltage control loop can maintain constant the output voltage and the output power across the entire range of possible input voltages. In the same model, load steps were also simulated. *Fig. 39* depicts the total output power for five different loads, and the secondary waveforms as a function of these load levels. This model's nominal power is 1.2 MW.
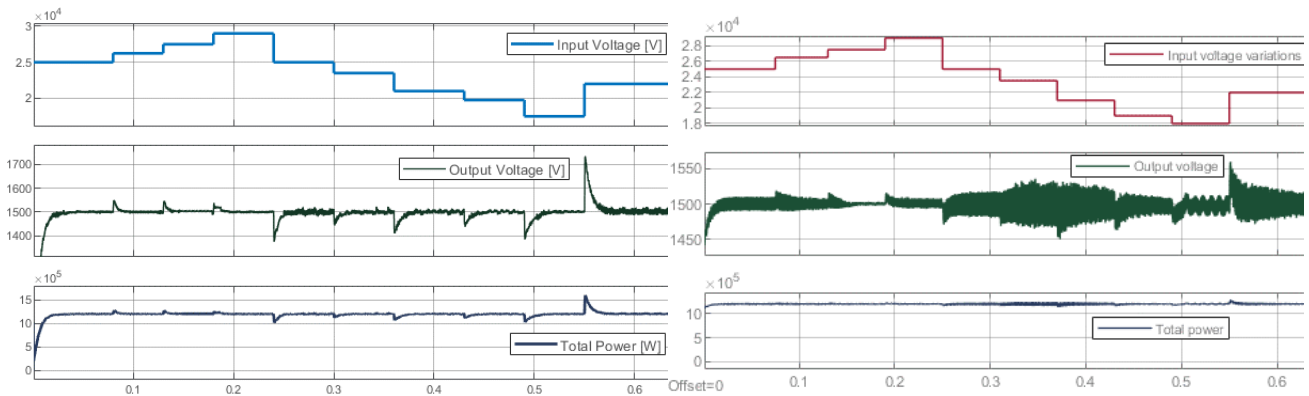
Fig. 38 – Ten different voltage levels from the lowest to the highest non-permanent catenary voltage. On the left side the simulation results of the BPSFB based system while on the right side for the DAB based system. The waveforms are Input voltage, output voltage (1500V nominal) and total power.
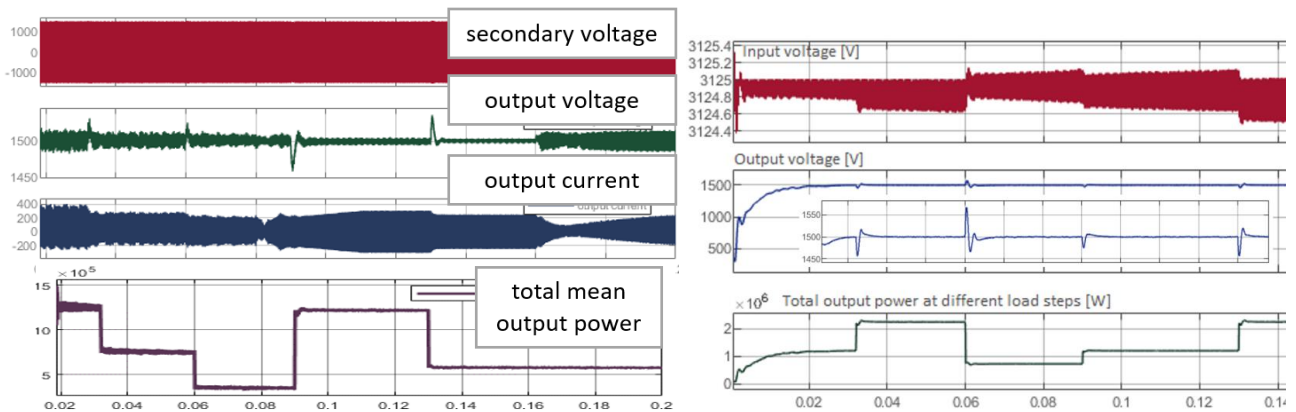

Fig. 39 – Secondary voltage, output waveforms and total output power at different load steps.

As seen on the figures above, the response of the system is satisfactory, and the output voltage is maintained at 1500 V with a transient voltage of less than 10 percent. The voltage ripple for both input voltage fluctuations and load steps is less than 5%. Both converters are a good solution for high-efficiency cascaded modular PETT for the future railway systems, it could be concluded. In addition, the new traction systems can be built with converter modules employing the most recent SiC or other WBG technologies to achieve high performance and power density [38]–[40]. There is a study about the advantages of WBG semiconductors in PETTs in [41]. Implementing a DC traction system for the new MVDC railway electrification concept is the novelty of this work [12]. The notion of replacing bulky and heavy line transformers with modular PETTs has been thoroughly explored and developed since 1985' [10], but it has always been limited to AC electrification systems [42].

Further details on losses, power density, efficiency and performance evaluation of both converters, as well as notes on zero voltage switching can be found in the thesis in the Findings section (4.5) of this chapter. Based on the performance evaluation of the DC PETT, it is conceivable to reach a power density of tens of MW/m^3 using SiC devices in modular MFT systems with a switching frequency of 10 to 20 kHz. Comparing the two converters, the DAB modules appear to be the simpler and more cost-effective choice for the traction system. Its applicability and performance were demonstrated using a full-scale software model across the entire range of catenary voltages. Both converter topologies and a brief literature research about power density and efficiency were utilized to validate the efficiency of the full-bridge topologies described in the previous chapter.

The following conclusions were derived as a result of building two somewhat different converter topologies as choices for the PETT modules, as stated in Table 9:

Table 9 – Comparison of DAB and BPSFB converters.

DAB converter	BPSFB converter
First order system: Simpler small signal model and easier to compensate (with a PI)	*Second order system*: More complex small signal model and regulator design, a PID may be necessary
Easier component design, leakage inductance can be integrated into the transformer	More complicated design procedure, output inductor can be difficult to design and integrate
It can be more compact	It may have higher volume then DAB, because of the output inductor
Easier to control the converter in forward and backward modes (both can be controlled with the phase shift only)	Forward and backward modes differ, also as small signal models, two different control mode is necessary, one for buck and one for boost mode
It can be more efficient at high power rates (no output inductor)	Efficiency may be limited, significant losses on output inductor at high power
Presents better cost-benefit ratio	Somewhat higher costs than DAB
ZVS can be obtained on the whole range of power	ZVS cannot be obtained on the whole range of power

Discussion and General Conclusions

This thesis is the product of a European Union project in collaboration with Shift2Rail and University of Birmingham, called Flexible MVDC-ERS. The PhD student from Technical University of Cluj-Napoca has been working on a major part of the 41 months project, related to the PETT of the proposed novel MVDC smart railway electrification line.

The objectives of the thesis (and the project) were to research and develop modern PETTs suitable for a new railway electrification system. In order to demonstrate the concept of the proposed rail network, detailed literature reviews, full-scale simulation models and experimental prototypes were developed for both the substation and the traction system by UoB and TUCN. This thesis successfully achieved the research objectives and the concept validation.

Thesis originality and personal contributions

The personal contributions brought by this work are:

1. Detailed literature research and comparative analysis of railway electrification systems, power electronic traction transformers and wide-band-gap semiconductors.

2. Definition of suitable topological families for DC power electronic traction transformers in the application of a novel medium voltage DC railway electrification smart network.

3. Proposal and analysis of two converter topologies for the modular traction system, including their controllers.

4. Mathematical modeling of the two topologies, including their control loop design.

5. Comparative analysis of three different snubber circuits for high-voltage spikes reduction. The study includes their mathematical model and design procedure as well.

6. Introduction of a regenerative active clamping snubber with a novel control mechanism, including its detailed mathematical model and design procedure.

7. Development of automated design sheets in Mathcad for both converter topologies.

8. Automated design sheet in Mathcad for the PI and PID controllers of the converter modules, using the frequency domain methods.

9. The full-scale simulation model of the DC power electronic traction transformer system and its simple control. The system was implemented in Matlab/Simulink with both converter topologies proposed and designed previously.

10. Implementing and testing experimentally the converter modules. The validation process was made through comparison of experimental results with simulation results, which were also compared with the values obtained in the Mathcad design sheet, using the mathematical model of the converters. Finally, the two topologies were compared.

List of Publications

WOS indexed papers:

- **I. Ferencz** and D. Petreuş, "Current Mode Control of a Solar Inverter with MPPT Algorithm," *2019 42nd International Spring Seminar on Electronics Technology (ISSE)*, 2019, pp. 1-7, doi: 10.1109/ISSE.2019.8810278.

- D. Petreuş, **I. Ferencz** and Z. Orbán, "Design of Regenerative Active Clamping Snubber for a Phase-Shift Converter," *2019 IEEE 25th International Symposium for Design and Technology in Electronic Packaging (SIITME)*, 2019, pp. 329-332, doi: 10.1109/SIITME 47687.2019.8990755.

- **I. Ferencz**, D. Petreuş and T. Pătărău, "Comparative Study of Three Snubber Circuits for a Phase-Shift Converter," *2020 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 2020, pp. 763-768,
doi: 10.1109/SPEEDAM 48782.2020.9161962.

- **I. Ferencz**, D. Petreuş, and P. Tricoli, "Converter Topologies for MVDC Traction Transformers," *2020 IEEE 26th Int. Symp. Des. Technol. Electron. Packag. (SIITME)*, 2020, pp. 362–367, 2020,
doi: 10.1109/SIITME50350.2020.9292214.

- **I. Ferencz**, D. Petreuş and P. Tricoli, "A power electronic traction transformer for a medium voltage DC electric railway system," *2021 44th International Spring Seminar on Electronics Technology (ISSE)*, pp. 1-6, 2021, doi:10.1109/ISSE51996.2021.9467646.

- **I. Ferencz**, D. Petreuş, "A Power Electronic Traction Transformer Model for a New Medium Voltage DC Electric Railway," *Advances in Electrical and Computer Engineering (AECE)*, vol.21, no.3, pp.99-108, 2021, doi:10.4316/AECE.2021.03012 – **Q3,** JCR Impact Factor: 0.825.

- **I. Ferencz**, D. Petreuş and T. Pătărău, "Small-Scale DC PETT Module Prototype for the Novel 25kV MVDC Electric Railway System," 2022 IEEE 16th International Conference on Compatibility, Power Electronics, and Power Engineering (CPE-POWERENG), 2022, pp. 1-6,
doi: 10.1109/CPE-POWERENG54966.2022.9880871.

- S. Sharifi, **I. Ferencz**, T. Kamel, D. Petreuş, P. Tricoli: Medium-voltage DC electric railway systems: A review on feeding arrangements and power converter topologies. IET Electr. Syst. Transp., vol. 12, issue 4, pp. 223-237, https://doi.org/10.1049/els2.12054, 2022. **Q2**, Impact Factor: **2.387**.

MVDC-ERS public project deliverables, available online at
https://projects.shift2rail.org/s2r_ipX_n.aspx?p=MVDC-ERS:

- **I. Ferencz**, "D2.1 – Converter topologies for MVDC transformers", 2020.

- **I. Ferencz**, "D2.2 – WP summary report – use of MVDC transformers for railway traction", 2022.

- S. Sharifi, **I. Ferencz**, "D4.2 Final project summary report", 2022.

Thesis Table of Contents

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